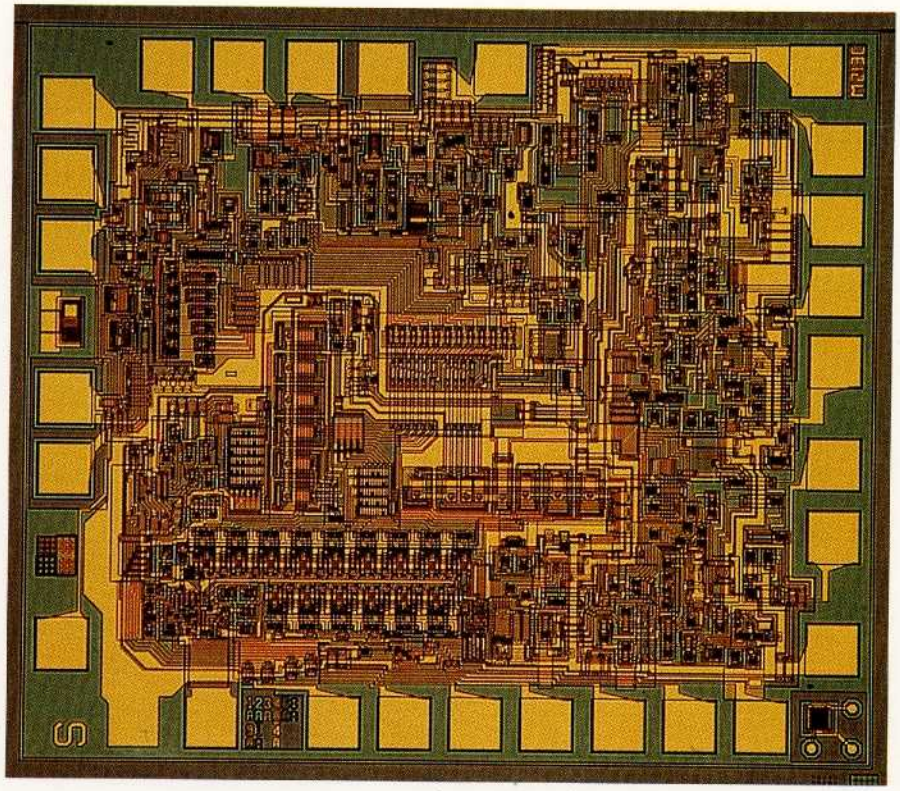
TEK-MADE INTEGRATED CIRCUITS CATALOG



Tektronix®
COMMITTED TO EXCELLENCE

COMPANY CONFIDENTIAL

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PURPOSE AND USE

This catalog contains integrated circuits that have had a Component Engineering Release by the publication date.

Data sheets are included for parts that are recommended for new designs. The data sheets, with a few exceptions, are intended to contain sufficient information so that a part may be designed into a new instrument design. For further applications information please call (phone 627-1037).

CORRECTIONS AND SUGGESTIONS

Corrections or suggestions for improvement are encouraged at any time. Mail to delivery station 59-355. A special form for this purpose is included in this catalog.

CATALOG DISTRIBUTION

Catalog distribution is automatic to all Electrical Engineers and E.E. managers. If you are not in this job category, please write to Applications Engineering, delivery station 59-355—include name, payroll code, and delivery station.

TEK-MADE I.C. QUESTIONNAIRE

We want to serve you better. If you are considering using a TEK-made I.C. for a new instrument design, we would like to hear from you.

I.C. Part Number _____

Do you need any additional information? Yes ☐ No ☐

Information Needed _____

Name _____

Delivery Station _____ Phone _____

Projected volume of new application _____ /yr

Approximate introduction date _____

Send to: ICM Application Engineering
Delivery Station 59-355

TEK-MADE I.C. QUESTIONNAIRE

We want to serve you better. If you are considering using a TEK-made I.C. for a new instrument design, we would like to hear from you.

I.C. Part Number _____

Do you need any additional information? Yes ☐ No ☐

Information Needed _____

Name _____

Delivery Station _____ Phone _____

Projected volume of new application _____ /yr

Approximate introduction date _____

Send to: ICM Application Engineering
Delivery Station 59-355

User Feedback

If we have slipped up and you feel there is room for improvement, please tell us at once. You will be doing us a great favor if you call a problem to our attention.

Your
Name _____ Address _____ Phone _____

ERRORS, OMISSIONS, SUGGESTIONS:

_____

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SEND TO: ICM APPLICATIONS ENGINEERING
D.S. 59-355

User Feedback

If we have slipped up and you feel there is room for improvement, please tell us at once. You will be doing us a great favor if you call a problem to our attention.

Your
Name _____ Address _____ Phone _____

ERRORS, OMISSIONS, SUGGESTIONS:

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SEND TO: ICM APPLICATIONS ENGINEERING
D.S. 59-355

TABLE OF CONTENTS

1

1

TABLE OF CONTENTS

1

TABLE OF CONTENTS (cont)

INDEX BY FUNCTION

NEW DESIGN CODE

P = Preferred
S = Suitable
X = Do Not Use

C = Call Application Engineering before using

155-XXXX = Packaged Parts
203-XXXX = Die

[a]not included in this catalog.

INDEX BY FUNCTION (cont)

Part Number Packaged Parts or Die	Description	New Design	Package Style	Page No.
	KNOB READOUT SYSTEM (cont)			
155-0087-00	Legend Generator	X	20 DIP	a
155-0088-00	Legend Generator	X	20 DIP	a
155-0104-00	Legend Generator	X	20 DIP	a
155-0105-00	Legend Generator	X	20 DIP	a
155-0110-00	Legend Generator	S	20 DIP	a
155-0135-00	Legend Generator	X	20 DIP	a
155-0171-00	4 Decade Counter and Memory	S	16 MINIPAC	a
155-0198-00	Knob Readout Counter	X	40 DIP	a
	READOUT SYSTEM			
155-0004-01	Beta Computer	X	16 DIP	a
155-0005-00	Beta Computer	X	16 DIP	a
155-0006-00	Beta Computer	X	16 DIP	a
155-0007-01	Readout I	X	16 DIP	a
155-0008-01	Readout II	X	16 DIP	a
155-0114-00	Seven Segment Character Generator	S	16 DIP	a
155-0119-00	Five Digit BCD Counter	X	40 DIP	a
	HORIZONTAL SYSTEM			
155-0028-00	Miller Integrator & Dly Pickoff	C	10 Lead TO-5	a
155-0028-01	Miller Integrator & Dly Pickoff	C	10 Lead TO-5	a
155-0048-01	Trigger & Sweep	P	16 MINIPAC	5-21
155-0049-02	Sweep Control	P	20 DIP	5-27
155-0055-00	Trigger & Sweep	P	16 DIP	5-35
155-0056-00	Sweep Control	C	16 DIP	a
155-0109-01	Trigger Circuit	P	16 DIP	5-61
155-0121-00	Trigger Subsystem	X	16 DIP	a
155-0122-00	Sweep Control	P	16 DIP	5-75
155-0123-00	Sweep & Pickoff	P	16 DIP	5-81
155-0124-00	Horizontal Preamplifier	P	16 DIP	5-87
155-0126-00	Trig Amp, Source Select	P	20 DIP	a
155-0151-00	Trigger Generator	X	20 DIP	a
155-0160-00	Trigger Amplifier, Source Select	C	16 MINIPAC	a
155-0196-00	Trigger Circuit	P	20 DIP	5-125
155-0216-00	Amplifier	S	16 DIP	a
155-0217-00	Amplifier	P	16 DIP	5-137
155-0241-00	Horizontal Amplifier	C	Power Pkg	a
203-0196-90	Horizontal Clamp	C		a
203-0213-90	600 MHz Trigger	P		6-43
203-0214-90	Sweep DAC & Logic	P		6-53
203-0229-90	300 MHz Trigger Amplifier	P		6-73
203-0231-90	Sweep Integrator	P		6-81

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INDEX BY FUNCTION (cont)

Part Number Packaged Parts or Die	Description	New Design	Package Style	Page No.
	DISCRETES			
151-0659-00	NPN Power Transistor	C	TO-39	a
151-1139-00	Dual FET	C	Special	a
152-0442-00	Schottky Diode	X	Special	a
152-0442-01	Schottky Diode Pair	X	Special	a
152-0446-00	Schottky Diode Pair	X	Special	a
152-0446-01	Schottky Diode Single	X	Special	a
152-0646-00	Schottky Diode Pair	C	Micro T	a
152-0646-02	Schottky Diode Pair	C	Micro T	a
203-0032-90	Schottky Diode	C	.....	a
203-0075-90	NPN Transistor	C	.....	a
203-0206-90	NPN Transistor	C	.....	a
203-0264-90	Schottky Diode	C	.....	a
203-0269-90	EBS Target Diodes	C	.....	a

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INDEX BY PART NUMBER

Part Number PACKAGED PARTS	Description	New Design	Page No.
131-1393-00	Programmed Connector	X	a
131-1394-00	Programmed Connector	X	a
131-1395-00	Programmed Connector	X	a
131-1396-00	Programmed Connector	X	a
131-1659-00	Programmed Connector	X	a
131-1660-00	Programmed Connector	X	a
151-0659-00	NPN Power Transistor	C	a
151-1139-00	Dual FET	C	a
152-0442-00	Schottky Diode Pair	X	a
152-0442-01	Schottky Diode Pair	X	a
152-0446-00	Schottky Diode Pair	X	a
152-0446-01	Schottky Diode Pair	X	a
152-0646-00	Schottky Diode Pair	C	a
152-0646-02	Schottky Diode Pair	C	a
152-0004-01	576 Readout System	X	a
155-0005-00	576 Readout System	X	a
155-0006-01	576 Readout System	X	a
155-0007-01	576 Readout System	X	a
155-0008-01	576 Readout System	X	a
155-0009-00	Horizontal Lockout Logic	S	a
155-0010-00	Chop Divider, Blanking	S	a
155-0011-00	Clock, Chop Blanking	S	a
155-0012-00	Z Axis Signal Conditioning	P	5-1
155-0013-00	Horizontal, Chop Alt Binary	S	a
155-0014-01	A/D Converter	S	a
155-0015-01	Data Switch	S	a
155-0017-00	Decade Counter	C	a
155-0018-00	Zero Logic	C	a
155-0019-00	Decade Counter	S	a
155-0020-00	Output Assembler	S	a
155-0021-01	Scan Osc. Logic Timing Gen.	S	a
155-0022-00	2 Input Channel Switch	P	5-7
155-0022-01	2 Input Channel Switch	S	a
155-0023-00	Character Generator	S	a
155-0024-00	Character Generator	S	a
155-0025-00	Character Generator	S	a
155-0026-00	Character Generator	S	a
155-0027-00	Character Generator	S	a
155-0028-00	Miller Integrator	C	a
155-0028-01	Miller Integrator	C	a
155-0031-01	Quad Timing Unit	X	a
155-0035-00	Quad Op. Amp.	P	5-11
155-0038-01	5-bit Precision D/A	S	a
155-0038-02	5-bit Precision D/A	P	5-17
155-0047-00	Dual Output Amplifier	S	a
155-0048-01	5 MHz Trigger and Sweep	P	5-21
155-0049-02	Sweep Control	P	5-27
155-0050-01	Vertical Preamp	S	a
155-0051-00	Z Axis, HV Regulator	S	a
155-0055-00	5 MHz Trigger and Sweep	P	5-35

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M Number vs. Package Part Number

	Packaged Part No./Die No.
M01A	155-0009-00
M04	155-0010-00
M12B	155-0011-00
M15B	155-0012-00
M18H	155-0028-00/01
M19F	155-0014-01
M20J	155-0015-01
M22	155-0013-00
M25E	155-0017-00
M26D	155-0018-00
M27B	155-0019-00
M28C	155-0020-00
M29B	155-0021-01
D32A	152-0646-00
M33B	155-0004-01
M34C	155-0005-00
M35B	155-0006-01
M36K	155-0022-00/01
M38C	155-0007-01
M39C	155-0008-01
M42D	155-0056-00
M45D	155-0038-01/02
M47	155-0031-01/
M50B	155-0047-00
M52G	155-0048-00, 155-0055-00
M53B	155-0035-00, 155-0116-00
M55E	155-0216-00, 155-0217-00
M65	155-0050-01
M68	155-0051-00
M77A	155-0059-00
M79H	155-0049-02
M80F	203-0080-90
M83	155-0061-00
M84F	155-0078-10, 155-0274-00
M89A	203-0089-91
M91E	155-0067-02
M94B	155-0076-00
M95A	155-0091-00
M96F	203-0096-90
M101B	155-0106-00
M105	155-0083-00
M112A	155-0198-00
D113C	155-0112-01
M115A	155-0199-00
M119	155-0110-00
M120D	155-0109-01
M121D	155-0126-00
M122C	203-0122-90
M123A	155-0119-00
M124A	155-0144-00

NEW DESIGN CODE

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C = Call Application Engineering before using

155-XXXX = Packaged Parts
203-XXXX = Die

M Number vs. Package Part Number (cont)

	Packaged Part No./Die No. (cont)
M126	203-0126-90
M127D	155-0114-00
M130	203-0130-90
M131A	155-0121-00
M132A	155-0122-00
M133A	155-0123-00
M136D	155-0160-00
M138	155-0124-00
M150A	155-0171-00
M151A	155-0145-00
M152D	155-0152-01
M154	155-0154-00
M155B	203-0155-91
M156	155-0288-00
M159	155-0151-00
M160A	155-0023-00
M161A	155-0024-00
M162A	155-0025-00
M163A	155-0026-00
M164A	155-0027-00
M165	155-0086-00
M166	155-0087-00
M167	155-0088-00
M169	155-0104-00
M170	155-0105-00
M171	155-0135-00
M175B	203-0175-90
M177A	203-0177-90
M178A	203-0178-90, 91, 92
M180D	155-0157-00
M181D	155-0158-00
M187A	155-0185-00
M188A	155-0196-00
M192C	155-0188-00
M196A	203-0196-90
M197A	203-0197-90
M198A	203-0198-90
M199A	203-0199-90
D206A	203-0206-90
M207	155-0187-00
M208	155-0205-00
M210C	203-0210-90
M211C	203-0211-90
M212C	203-0212-90
M213C	203-0213-90
M214C	203-0214-90
M215E	155-0241-01
M216C	203-0216-90
M217G	155-0244-00
M218A	155-0215-00

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155-XXXX = Packaged Parts
203-XXXX = Die

M Number vs. Package Part Number (cont)

	Packaged Part No./Die No. (cont)
M222B	155-0218-00
M223B	155-0247-00
M227C	203-0227-90
M228B	155-0279-00, 155-0283-00
M229C	203-0229-90
M231B	203-0231-90
M232B	155-0277-00
M234B	155-0253-00
M240	203-0240-90
M241B	155-0280-00
M274B	203-0274-90
M289A	155-0273-00
M297A	203-0297-90
M307B	203-0307-90
M312A	155-0282-00

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203-XXXX = Die

NEW DESIGN INFORMATION 2

2

Preferred for New Designs—Cost Effective or State-of-the-Art

[a]not included in this catalog.

Suitable for New Designs—Older Still Useful Parts

Packaged Parts

155-0009-00	Horizontal Lockout Logic
155-0010-00	Chip Divider, Blanking
155-0011-00	Clock Chop Blanking
155-0013-01	Horiz Chop Alt Binary
155-0014-01	A/D Converter
155-0015-01	Data Switch
155-0019-00	Decade Counter
155-0020-00	Output Assembly
155-0021-01	Scan Osc. Logic Timing Generator
155-0022-01	Channel Switch
155-0023-00	Character Generator
155-0024-00	Character Generator
155-0025-00	Character Generator
155-0026-00	Character Generator
155-0027-00	Character Generator
155-0038-01	D/A Converter
155-0047-00	Dual Output Amplifier
155-0050-01	Vertical Preamp
155-0051-00	Z-axis, HV Regulator
155-0059-00	Gain Trim Amplifier
155-0061-00	F_t Doubler Amplifier
155-0083-00	Dual Op Amp, Current Source
155-0091-00	250 MHz Channel Switch
155-0110-00	Legend Character
155-0114-00	7 Segment Character Generator
155-0171-00	4 Decade Counter Memory
155-0185-00	4 Decade DVM
155-0187-00	F_t Doubler
155-0216-00	Amplifier

Die

203-0080-90	Vertical Output Amplifier
203-0126-90	F_t Doubler

Do Not Use for New Designs—Obsolete Designs, Replaced by Newer Designs, or No Longer a Process in Production

Packaged Parts

131-1393-00	Programmed Connector
131-1394-00	Programmed Connector
131-1395-00	Programmed Connector
131-1396-00	Programmed Connector
131-1659-00	Programmed Connector
131-1660-00	Programmed Connector
152-0314-00	Schottky Diode
152-0442-00	Schottky Diode
152-0442-01	Schottky Diode Pair
152-0446-00	Schottky Diode Pair
152-0446-01	Schottky Diode Single
155-0004-01	576 Readout System
155-0005-00	576 Readout System
155-0006-01	576 Readout System
155-0007-01	576 Readout System
155-0008-01	576 Readout System
155-0031-01	Quad Timing Unit
155-0087-01	Quad Timing Unit
155-0088-00	Legend Character
155-0104-00	Legend Character
155-0105-00	Legend Character
155-0106-00	Normalizing Circuit
155-0111-01	LED Array
155-0112-01	Photo Transistor Array
155-0119-00	5-Digit BCD Counter
155-0121-00	50 MHz Trigger
155-0135-00	Legend Character
155-0151-00	100 MHz Trigger
*155-0157-00	MOS Digital Storage Vertical Control
*155-0158-00	MOS Digital Storage Horizontal Control
*155-0198-00	MOS Knob Readout Counter
*155-0199-00	MOS Vertical Control
155-0205-00	F_t Doubler
*155-0207-00	Vertical Output
206-0186-06	Transistor Temperature Probe
206-0286-11	Transistor Temperature Probe

Die

203-0096-90	Logic Probe
203-0268-90	PNP Transistor
203-0276-90	50 Ohm Resistor
203-0290-90	Schottky Diode

***Limited supply—process capability does not exist.**

Call Application Engineering Before Using

Packaged Parts

151-0659-00	NPN Power Transistor
151-1139-00	Dual FET
152-0646-00	Schottky Diode Pair
152-0646-02	Schottky Diode Pair
155-0017-00	Decade Counter
155-0018-00	Zero Logic
155-0028-00	Miller Integrator
155-0028-01	Miller Integrator
155-0056-00	Sweep Control
155-0076-00	Input Protection
155-0160-00	Trigger Source/Amplifier
155-0241-00	Horizontal Amplifier

Die

203-0032-90	Schottky Diode
203-0075-90	NPN Transistor
203-0088-90	Vertical Amplifier
203-0122-90	1 GHz Trigger
203-0130-90	100 MHz Vertical Preamp
203-0175-90	Dual Comparator
203-0178-90	1 GHz Vertical Amplifier
203-0196-90	Horizontal Clamp
203-0197-90	Horizontal Output
203-0198-90	Clamp & Sensor
203-0199-90	1 GHz Input Amplifier
203-0206-90	NPN Transistor
203-0210-90	300 1MHz Vertical Preamp
203-0264-90	Schottky Diode
203-0269-90	EBS Target Diodes
203-0270-90	NPN 3 Watt 2 GHz Transistor
203-0271-90	NPN 5 Watt 150 V .5 GHz Transistor
203-0265-90	Schottky Diode
203-0266-90	Schottky Diode

Q.A. PROGRAM

3

3

ICM QUALITY

3

QUALITY POLICY

Integrated Circuits Manufacturing exists to provide quality products and services to our customers on time at reasonable cost. Quality is meeting all the requirements of the "specification". The standard of performance is complete conformance to the requirements for guaranteed customer satisfaction. Any change in requirements must be officially documented and reflect what we and our customers really need.

Our intent is that quality be built into each product during the design, development, and manufacturing stages of product life. Defect prevention, rather than "inspecting" quality in, is to be emphasized at all times at all organizational levels. Each individual is responsible for the quality of his/her work, and each manager is responsible for the quality of work performed under his/her direction. Correction of major plant and field problems will be given prompt attention and timely resolution.

3

MANUFACTURING, SCREENING AND INSPECTION for INTEGRATED CIRCUITS

The following flow chart describes the major process steps and the key quality check points for producing hermetic and molded package I.C.'s. All operations are totally specified in product, process, test, and quality assurance specifications.

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

I

INCOMING INSPECTION

Starting materials are inspected for conformance to specified requirements. Inspection follows written procedures and records are to establish suppliers quality ratings.

II

WAFER FABRICATION

a

Repeated masking, etching, and diffusion processes produce finished die in wafer form. All processes are monitored on process control charts.

IN-PROCESS INSPECTION

b

Each wafer is inspected prior to irreversible process steps. Special capacitance vs. voltage tests (CV Monitor) are performed regularly to prevent inversion. A scanning electron microscope (SEM) is used to check metal step coverage and metalization integrity. A PSG (Phospo-silicate glass) monitor checks phosphorous content of the passivation.

c

FINISHED WAFER INSPECTION

A computerized test station electrically probes test elements on all lots to guarantee electrical performance at die sort. All wafers are visually process inspected and then audited by Q.A. to a 2.5% AQL. All lot data is verified for completeness.

= Process step
= In-process inspection
= Off line quality inspection

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

III

DIE SORT
WAFER ELECTRICAL TEST

a Electrical probe test is done on 100% of the die to component specifications. A computer controlled test system measures functional parameters and identified die that do not meet electrical requirements.

b **QUALITY INSPECTION**

All wafers are visually inspected and wafer maps are verified to the marked wafer.

IV

DIE PREP
SAW AND SEPARATE

a Wafer is sawn into individual die and electrical rejects are removed. Separated die are 100% inspected and selected at high magnification.

b **QUALITY INSPECTION**

Die are visually sampled by Q.C. and again by Q.A. inspectors (1% AQL). All product lot data verified.

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

V

ASSEMBLY

a — Die are attached, wirebonded, and sealed (or encapsulated) in a designated package. Die attach is performed with conductive epoxy. Strength is confirmed by push testing samples. Thermosonic gold wire bonding is the primary bonding process. Bond strength is sampled on all lots.

IN-PROCESS INSPECTION

b — The die position and visual quality of epoxy flow is confirmed on all lots. The wire bond size, location, wire dress, and general workmanship is inspected.

QUALITY INSPECTION

c — Prior to sealing, all units are inspected at high and low power.

FINAL SEAL

d

(Hermetic devices: Metal Cans, Ceramic packages)

ENCAPSULATE

e

(Molded devices: Dual-In-Line packages)

AGE (STABILIZATION BAKE)*

f — Encapsulated devices are baked at 150°C for 16 to 65 hours to stabilize mobile ions.

TEMPERATURE CYCLE*

g — All parts are cycled 15 times between −55° and +125°C to screen out marginal parts.

HERMITICITY*

h — Fine leak and gross leak checks are given all hermetic packages.

CLEAN AND MARK

i — Part number, lot code, and date codes are marked on the package.

QUALITY INSPECTION

j — A visual confirmation of marking and physical quality is completed. A check on documentation and a completion of process requirements is done.

RELIABILITY SCREENS

* Reliability Screens

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

VI

FINAL TEST

a. 100% of parts tested to requirements of component specifications: Includes static, dynamic, and functional tests specified temperatures.

QUALITY INSPECTION

b. Visual confirmation of marking and physical quality. Electrical confirmation of product identity by sample test to a 0.65% AQL. Confirmation of completion of all process steps and required documentation.

SHIP TO WAREHOUSE

c. Specialized reliability assurance screen tests, such as burn-in, can be developed for a specific application to insure a product's reliability. Initial discussions should be coordinated with an Applications Engineer. Quality and Reliability Engineers are also ready to support you and your application.

3

RELIABILITY

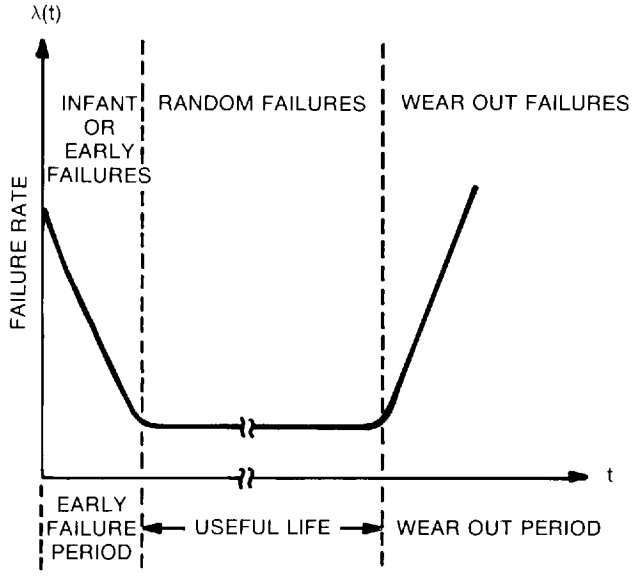
4

4

RELIABILITY

The reliability of a circuit component is the probability of failure-free performance of a required function under stated conditions for a given period of time. It is possible to calculate the probability of successful operation to a specified confidence interval.

The typical failure rate behavior of a device is shown in the figure below:



INFANT MORTALITY: Early in the lifetime of a device there can be a relatively large number of failures, due to built-in weakness or defect. These early failures show a decreasing failure rate with respect to a relatively short time period.

USEFUL LIFE: During the middle period of the device lifetime fewer failures occur but it is necessary to know which failure mechanism is the principal determinant of the failure rate under the conditions of interest. In this region, sometimes called the "random failure region" of constant failure rate, the device characteristics are essentially constant and when failure occurs it is usually catastrophic.

WEAR-OUT REGION: As a device reaches the age at which wear-out failure mechanisms are activated it begins to deteriorate rapidly. The instantaneous failure rate increases monotonically and many failures occur. This failure region is called the "wear-out region" and is caused by material degradation, effect of electrical fields, and slow chemical reactions. Integrated circuits do not usually reach the wear-out region in normal operation. Exceptions occur when integrated circuits are exposed to ionizing radiation fields and when the hermeticity of integrated circuit packages is impaired by progressive corrosion. An "intrinsic" wear-out process leads to the ultimate failure of every device.

INTEGRATED CIRCUIT FAILURE MECHANISMS

The physical or chemical process that causes devices to fail is termed the *failure mechanism.* The cause of rejection of any failed device is termed the *failure mode.* Thus, electromigration is an example of a failure mechanism, which can lead to the failure mode of an open interconnection. A further example is given by excess charge near a silicon-oxide interface (failure mechanism) which causes drift of the parameters of a MOS transistor (failure mode).

Failure mechanisms for bipolar integrated circuits can be divided roughly into three groups, namely: (1) die-related failures, such as oxide defects, metallization defects, and diffusion-related failures; (2) assembly-related problems such as die mount, wire bonds, or package failures; and (3) miscellaneous undetermined, or application-induced failures.

DIFFUSION-RELATED FAILURES: Nonuniform current-flow may occur within a device because of dopant diffusion-related causes. These may affect the base width, the emitter resistivity, the curvature of junctions, and other device parameters.

OXIDE-RELATED FAILURES: Contamination of oxide, during or after its growth, directly affects its dielectric properties, particularly its breakdown strength. Presence of surface charge, Q_{SS}, at or near an oxide-silicon interface can affect the turn-on voltage, V_{TH}, of a device and other parameters, such as dc gain, and leakage current. Oxide-charge values of large magnitude can cause surface inversion. Other surface-related failures arise because of ion migration in the thermally grown oxide and along its surface, dipole polarization effects or charge trapping effects.

METALLIZATION-RELATED FAILURES: The mass transport of metal atoms by momentum exchange with conducting electrons is called "electromigration". It occurs in metal lines at high current densities and elevated temperatures, and consists of the movement of metal atoms toward the positive end of the conductor, while voids move in the opposite direction. As a consequence, metal disappears from certain regions and ultimately an open-circuit occurs. The degradation of integrated circuits with aluminum metallization operating at high current densities and at elevated temperatures is described by the Arrhenius model. Electromigration occurs for many metals, including aluminum, gold, silver, copper, and platinum. The current density at which reliability problems occur with gold films is substantially higher than that for aluminum films. This has led to the use of gold in circuits requiring high current densities.

Another significant cause of metallization failure is the formation of microcracks, where the metallization passes over an oxide step. It occurs frequently where the oxide step is greater than 6000 Angstrom. Steeper steps lead to thinner metal deposits which have a greater probability of failure under high current stress. Microcracks are not usually detectable with optical microscopes, but may effectively be detected by scanning electron microscopes.

Metallization may also fail because of poor ohmic contacts with silicon, poor bondability to aluminum or gold wires, or poor adhesion to the silicon dioxide.

DIE MOUNT FAILURES: Die to leadframe attachment failures have been attributed to low strength adhesion caused by inadequate process control. Epoxy mounts may fail under temperature stress because the thermal coefficient of expansion of most epoxies exceeds the coefficients of expansion of both the semiconductor die and the leadframe to which it is mounted.

WIRE BOND FAILURES: Gold wire is bonded to the die metallization. Failure of gold wire bonds to aluminum-metallized die may be due to the formation of intermetallic compounds that lead to loss of strength and an increase of resistance.

PACKAGE-RELATED FAILURES: The hermeticity of metal can packages depends on a glass to metal seal that isolates the leads going to the device. The coefficient of expansion is matched to that of the header. Failure may occur due to poor hermeticity due to corrosion of the header.

Plastic packages are formed by molding the device in molten plastic. Failure is usually due to environmental factors; however, with proper design and testing they have a high degree of reliability.

EARLY FAILURES—RELIABILITY SCREENING PROCEDURES

Ideally, reliability screening selects from a lot of devices having superior reliability and rejects those devices that are potential early failures. Assuming that all devices in a lot are intitially within specification, screening is a test procedure that classifies a device as to longevity, based on time-zero or short-time measurements. See the Quality Assurance section flowchart for a description of the reliability screens performed on all parts.

Specialized additional reliability assurance screen tests such as burn-in, are available for your specific applications. Initial discussions should be with an Applications Engineer.

ACCELERATED-STRESS LIFE TESTING

The purpose of a life test is to be able to predict device reliability when the device is operating in a specified environment. Frequently, a device is so reliable under normal operating conditions that years of testing would be required in order to predict its reliability. Hence, there exists a great difficulty, because the greater the reliability of a device, the more difficult it is to determine this reliability.

A solution to this dilemma is to design accelerated-stress life tests in which a device is run at a higher stress level than encountered in normal operation. As a consequence, the device has a shorter life than under normal conditions. Results obtained at more severe stress levels are then extrapolated to normal stress levels so as to obtain an estimate of the life distribution. Accelerated-stress testing typically employs higher than normal temperature as the stress mechanism. The Arrhenius equation to relate the failure rate at one temperature to that at a different temperature is:

$$\text{Acceleration Factor} = e^{\frac{Ea}{k}\left[\left\{\frac{1}{T_1 + 273} - \frac{1}{T_2 + 273}\right\}\right]}$$

in which Ea = activation energy for the failure mechanism

k = Boltzman constant 8.62×10^{-5} EV/°C

T_1 = Reference temperature in °C

T_2 = Stress temperature in °C

NEW PRODUCTS AND PROCESSES

New products and processes are evaluated for reliability before they are transferred to regular production. New circuits, packages and process test devices are subjected to the rigorous electrical and mechanical tests listed below in Table I.

TABLE I

TEST	STRESS	PURPOSE
Mechanical Shock	15 g for .5 sec.	The shock test is intended to determine the suitability of the device for use in equipment that may be subjected to moderately severe shocks encountered in rough handling, transportation or field operation.
Vibration	20 g; 20-1000 cycles	The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range.
Lead integrity	Lead pull Lead bend Stud Torque	This test provides various tests to determine the integrity of device leads, welds, and seals.
Thermal Shock	−55°C to +125°C 100 cycles +20°C to +260°C 10 cycles	The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature.
Humidity	−10°C to +65°C Relative humidity of 95% to 98% 10 cycles of 24 hours each.	This test is performed to evaluate in an accelerated manner the resistance of the part to the effects of high humidity.
High Temperature Storage	150° for 60 hours	This test is to determine the effect on the device of storage at high temperature without electrical stress applied.
High Temperature Operating Life	Static and dynamic operating life tests at a junction temperature of 150°C.	This life test is performed for the purpose of determining a representative failure rate.

ON-GOING RELIABILITY MONITOR

A Reliability Assurance Monitor program is established that regularly runs accelerated life tests on samples from production output. This monitor is our assurance that integrated circuits continue to maintain their high reliability.

The part numbers for the Reliability Assurance Monitor have been classified according to process and package types. Accelerated life tests are scheduled so that during any period of time, a number of production samples of each classification are on life test. The part numbers run during a year represent 90% of the output volume of Integrated Circuits Manufacturing.

4

PACKAGED PARTS (DATA SHEETS)

5

SECTION 5 PACKAGED PARTS (DATA SHEETS)

PREFERRED FOR NEW DESIGNS—COST EFFECTIVE OR STATE-OF-THE-ART

"Z" AXIS LOGIC

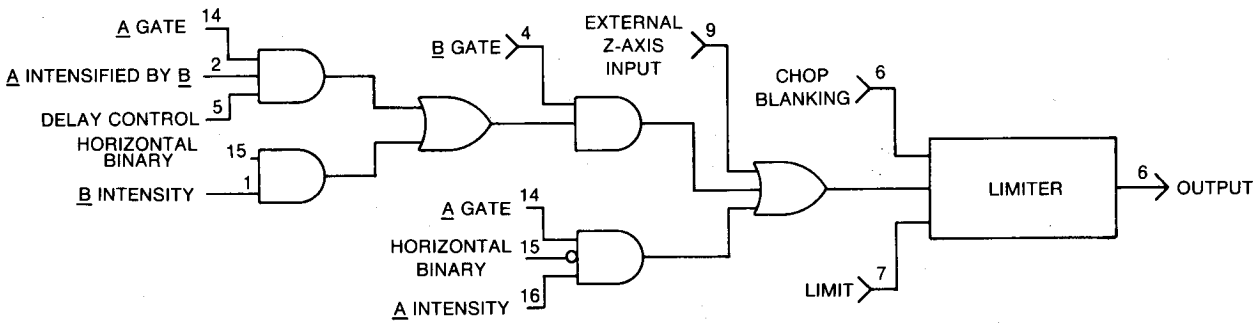
DESCRIPTION

The 155-0012-00 is a Z-axis logic control circuit. The part is under the control of the horizontal switch drive. It properly selects A intensity or A intensified by B.

FEATURES

- 4 current inputs
- 1 current output
- 4 logic inputs
- Chopped blanking
- Fast limiting of composite signal.
- Slow sweep speed limiting to prevent CRT phosphor burn.

BLOCK DIAGRAM



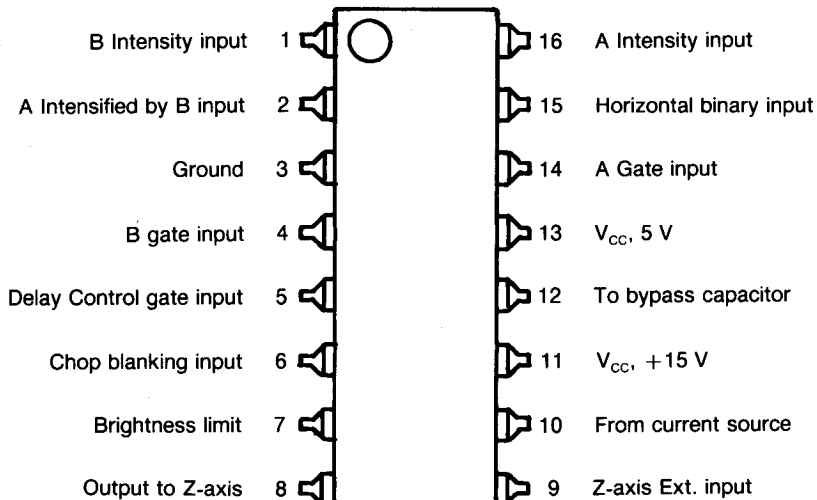
5

ABSOLUTE MAXIMUMS

Environmental

Symbols	Identifications	Values	Units
T_{stg}	Storage temperature, range.	−55 to +125	°C
T_A	Operating ambient temperature, range.	0 to +70	°C

PIN CONNECTIONS



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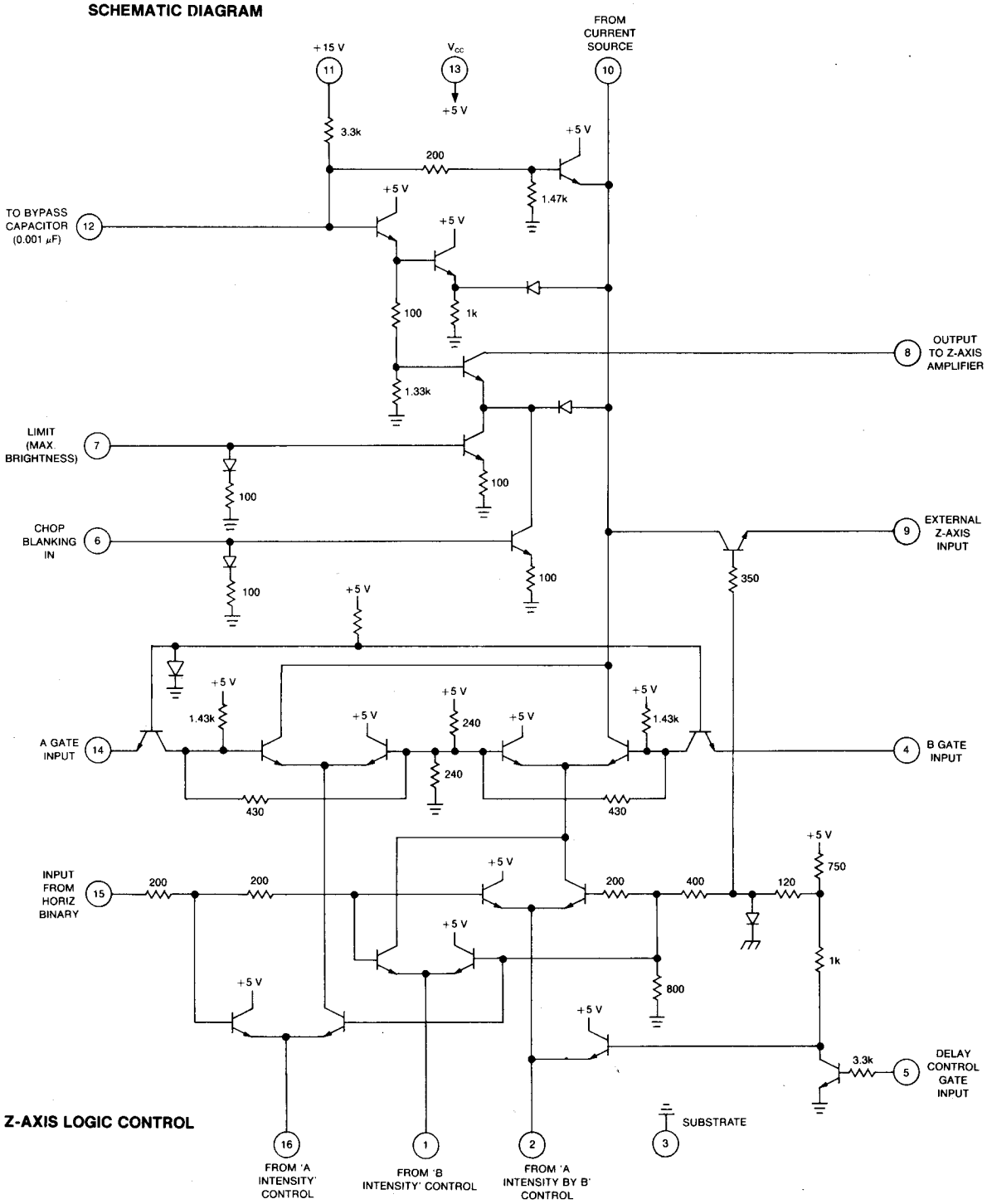
SCHEMATIC DIAGRAM



Z-AXIS LOGIC CONTROL

5

ELECTRICAL CHARACTERISTICS

PIN #'s	IDENTIFICATION	NOTES AND TEST CONDITIONS	MIN	MAX	UNITS
Pin 4	B gate; current	Logical 0	2.3		mA
Pin 4	B gate; current	Logical 1		0.5	mA
Pin 5	Delay control; voltage	Logical 0		0.600	V
Pin 5	Delay control; voltage	Logical 1	0.8		V
Pin 14	A gate; current	Logical 0	2.3		mA
Pin 14	A gate; current	Logical 1		0.5	mA
Pin 15	Horizontal binary; voltage	Logical 0		0.2	V
Pin 15	Horizontal binary; voltage	Logical 1	0.7		V
Pin 14	Output (pin 8) risetime; input at A gate (pin 14)			4.6	ns
Pin 4	Output (pin 8) risetime; input at B gate (pin 4)			3.9	ns
Pin 6	Output (pin 8) risetime; input at chop blanking (pin 6)			2.6	ns
Pin 9	Output (pin 8) risetime; input at external input (pin 9)			3.3	ns
Pin 14	Output (pin 8) falltime; input at A gate (pin 14)			4.2	ns
Pin 4	Output (pin 8) falltime; input at B gate (pin 4)			3.6	ns
Pin 6	Output (pin 8) falltime; input at chop blanking (pin 6)			2.3	ns
Pin 9	Output (pin 8) falltime; input at external input (pin 9)			1.4	ns
Pins 14-8	Propagation delay, A gate input (inverting)	For negative-slope input transition		1.9	ns
Pins 4-8	Propagation delay, B gate input (inverting)	For negative-slope input transition		1.3	ns

ELECTRICAL CHARACTERISTICS (cont)

PIN #'s	IDENTIFICATION	NOTES AND TEST CONDITIONS	MIN	MAX	UNITS
Pins 6-8	Propagation delay, chop blanking input (inverting)	For negative-slope input transition		1.4	ns
Pins 9-8	Propagation delay, external input (noninverting)	For negative-slope input transition		2.9	ns
Pins 14-8	Propagation delay, A gate input (inverting)	For positive-slope input transition		4.0	ns
Pins 4-8	Propagation delay, B gate input (inverting)	For positive-slope input transition		6.5	ns
Pins 6-8	Propagation delay, chop blanking input (inverting)	For positive-slope input transition		4.4	ns
Pins 9-8	Propagation delay, external input (noninverting)	For positive-slope input transition		0.94	ns
h_{fb} Pins 16-8	Current gain from A intensity input	I = 1.0 mA and I = 5.0 mA	.87	1.01	
h_{fb} Pins 1-8	Current gain from B intensity input	I = 1.0 mA and I = 5.0 mA	.87	1.01	
h_{fb} Pins 2-8	Current gain from A intensified by B input	I = 1.0 mA and I = 5.0 mA	.87	1.01	
h_{fb} Pins 9-8	Current gain from external input	I = 1.0 mA and I = 5.0 mA	.89	1.01	
h_{fb} Pins 6-8	Current gain from chop blanking	I = 1.0 mA and I = 5.0 mA	.92	1.01	
h_{fb} Pins 7-8	Current gain from limit	I = 1.0 mA and I = 5.0 mA	.92	1.01	

Reliability

λ, failure rate $\leq$.02%/1K hours at 75°C Tj

5

CHANNEL SWITCH

DESCRIPTION

This monolithic integrated circuit selects one or mixes two input analog signals in response to a digital input.

High speed switching between two inputs for "CHOPPED" or "ALTERNATE" operation is possible to frequencies of 1 MHz.

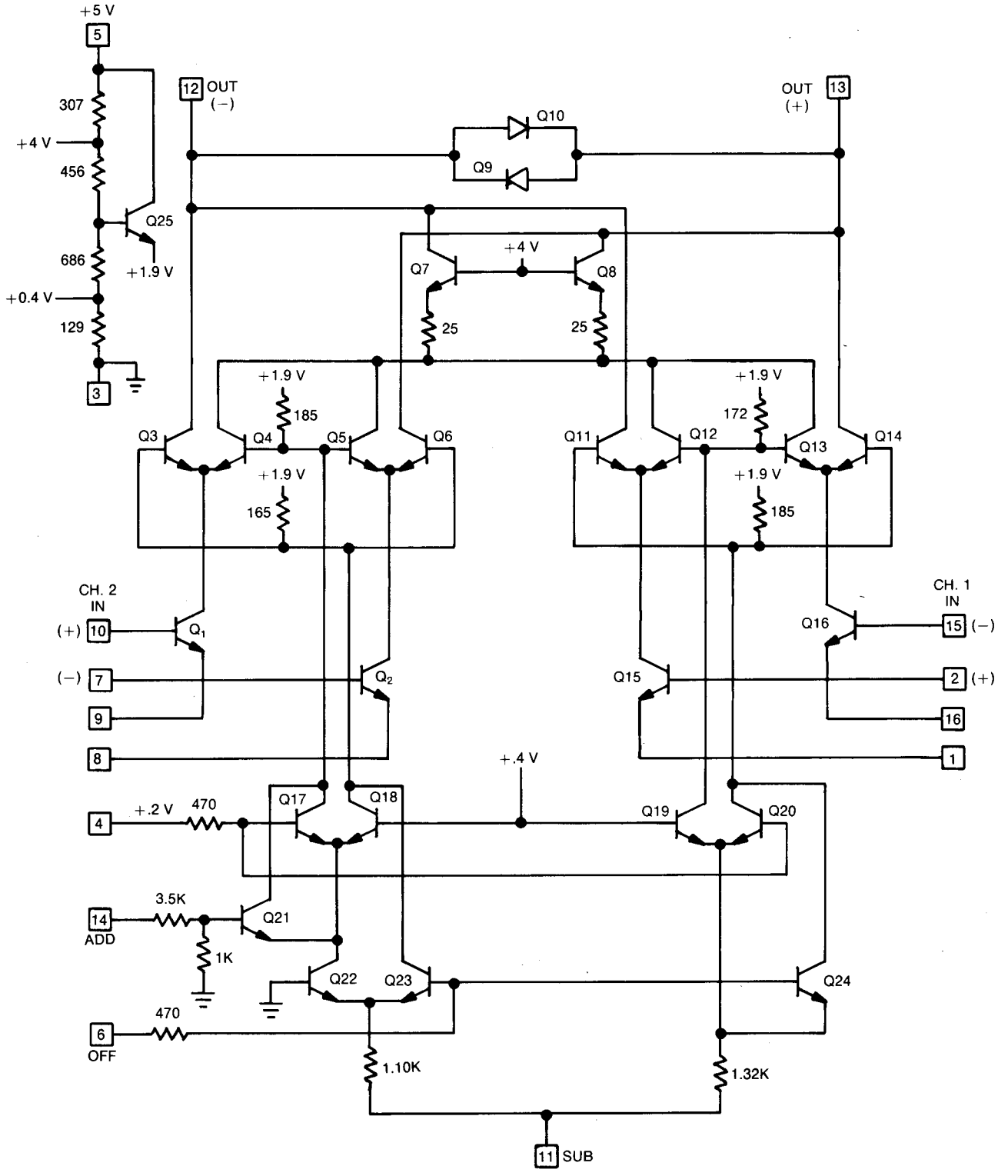
FEATURES

- Signal rise time <2.5 ns.
- Output current swing ±7.5 mA MAX
- Output impedance 100 KΩ NOM
- Input capacitance 2.3 pF NOM
- Output capacitance 5.2 pF NOM
- Differential DC offset between modes 20 mV MAX

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
T_{STG}	Storage temperature, range	−55 to +125	°C
T_a	Operating ambient temperature range	0 to +70	°C
	Maximum voltage at pins 12 and 13 (referred to pin 3)	+10	V
	Maximum (negative) voltage at pin 11 (referred to pin 3)	−10	V

SCHEMATIC


+5 V
5
307
+4 V
456
686
+0.4 V
129
3
12 OUT (−)
OUT (+) 13
Q10
Q9
Q25
+1.9 V
+4 V
Q7
Q8
25
25
+1.9 V
185
Q3
Q4
Q5
Q6
+1.9 V
165
+1.9 V
172
Q11
Q12
Q13
Q14
+1.9 V
185
CH. 2 IN
(+) 10
Q1
(−) 7
Q2
9
8
CH. 1 IN
Q16
15 (−)
Q15
2 (+)
16
1
+.4 V
+.2 V
470
4
Q17
Q18
Q19
Q20
3.5K
14
ADD
Q21
1K
Q22
Q23
Q24
470
6
OFF
1.10K
1.32K
11 SUB

ELECTRICAL CHARACTERISTICS

(For an ambient temperature of 25°C unless otherwise noted.)

SYMBOLS	IDENTIFICATION	NOTES AND TEST CONDITIONS[1]	VALUES MIN	VALUES MAX	UNITS
V_{L4}	CH 1—Ch 2 switch input, pin 4 voltage. See note 7.	LOW — CH 1 on:	−0.5	+0.2	V
V_{H4}		HIGH—CH 2 on;	+0.6	+1.0	V
V_{L14}	ADD switch input, pin 14 voltage. See note 7.	LOW—Non-add:	−0.5	+1.0	V
V_{H14}		HIGH—Add	+4.0	+5.0	V
V_{L6}	OFF switch input, pin 6 voltage. See note 7.	LOW—on:	−0.5	−0.2	V
V_{H6}		HIGH—off:	+0.5	+1.0	V
Ai	Current gain	See note 2	1.00	1.14	
Io_{MAX}	Output dynamic range	See note 3	−7.5	+7.5	mA
ΔV_{OFFSET}	DC offset between modes	See note 4		12	mV
V_{OFFSET}	DC offset in any mode	See note 4		50	mV
ϵ_{ADD}	ADD mode error	See note 5		1.0	%
I_{IN2}	Input current; Pin 2	Connected as shown. Voltage on Pins 2, 15, 7, and 10 held at 0 V. Pin 14 to +5 V. Implies beta = 60		.125	mA
I_{IN15}	Input current; Pin 15			.125	mA
I_{IN7}	Input current; Pin 7			.125	mA
I_{IN10}	Input current; Pin 10			.125	mA
T_r	Risetime (CH 1 to OUTPUT; then CH 2 to OUTPUT) See note 6	Connect device as shown.		<2.5	ns

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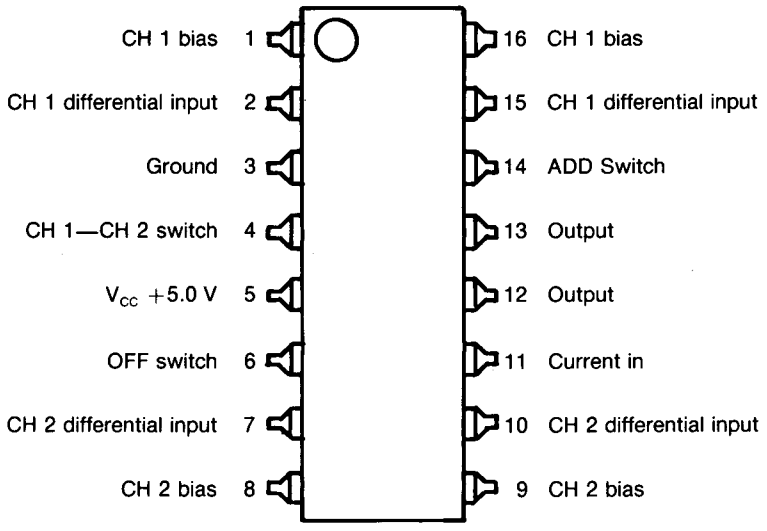
PIN CONNECTIONS



APPLICATIONS

In its simple application, the 155-0022-00 is a double-pole, double-throw selector of one of two balance input signals. Its more sophisticated role is in providing signal steering in dual-trace vertical and horizontal amplifiers.

It is designed for two balanced input signals of 25 mV/division per side into 50 Ω terminations to ground are external to the package. A current gain of "1" is intended.

The switch output is at or slightly above a +5 volt DC level. It is a current output into a resistance of 50 Ω per side. Side-to-side diodes are included inside the circuit for limiting the differential voltage swing of the output.

The OFF input turns both inputs "off". The ADD input turns both inputs "on". The common mode current output of the signal channel is maintained and constant for the various modes.

RELIABILITY

λ, Failure rate ≤0.02%/1K hours at 75°C T_j

QUAD OPERATIONAL AMPLIFIER

DESCRIPTION

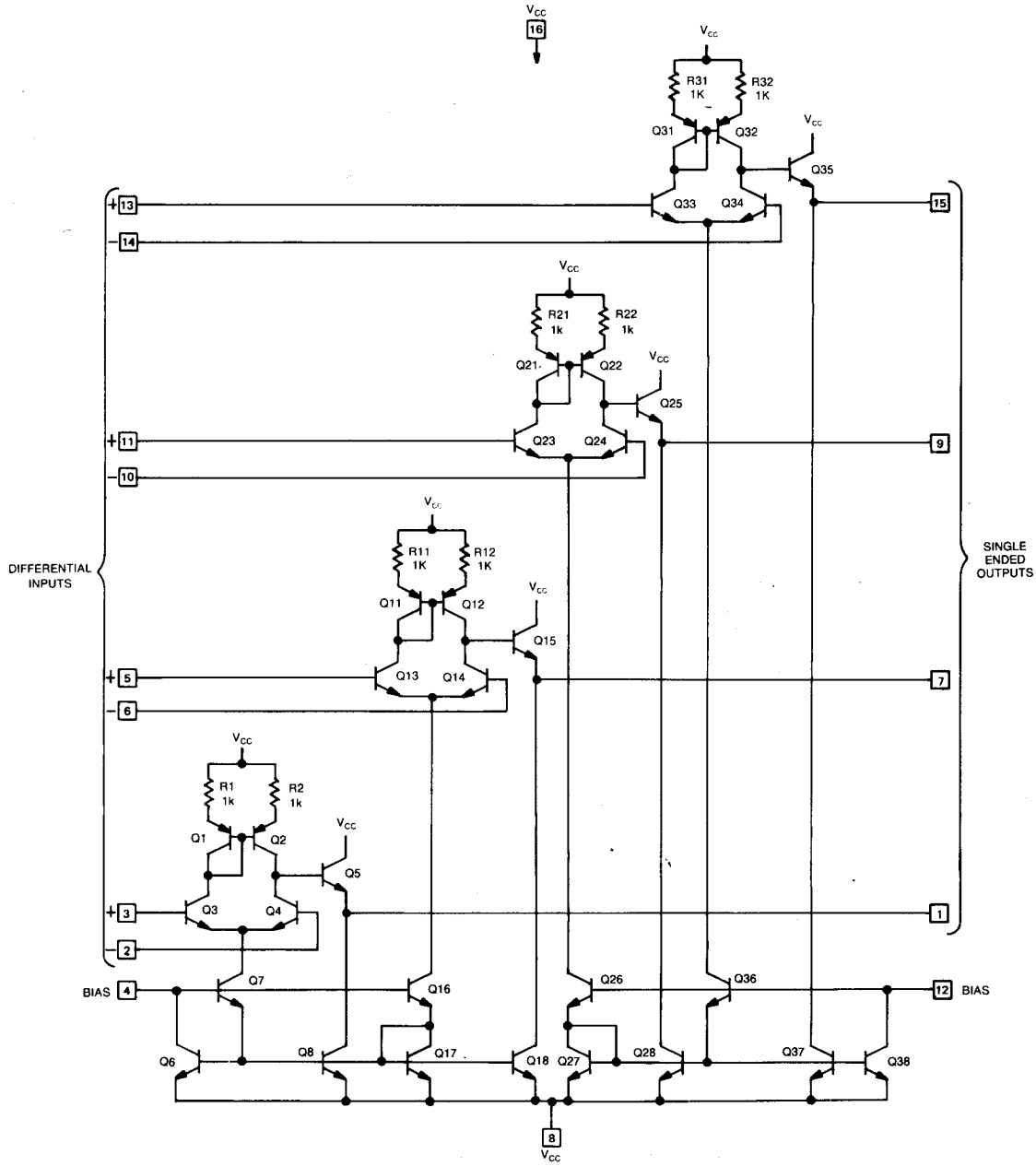
The 155-0035-00 is a silicon monolithic quad operational amplifier. It comes in a plastic 16 pin package.

FEATURES

- ±5 volt to ±15 volt power supply range.
- 80 MHz gain bandwidth product.
- 20 mA output bandwidth product.
- No compensation required.
- Open loop gain 3300 typical.
- 5 mV input offset voltage.
- Available in two versions:

  155-0035-00 (plastic DIP)
  155-0116-00 (ceramic DIP)

SCHEMATIC



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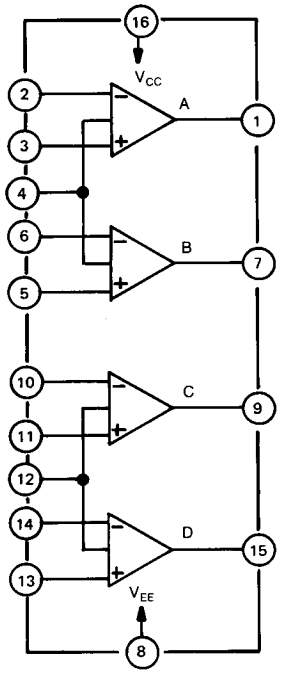
BLOCK DIAGRAM

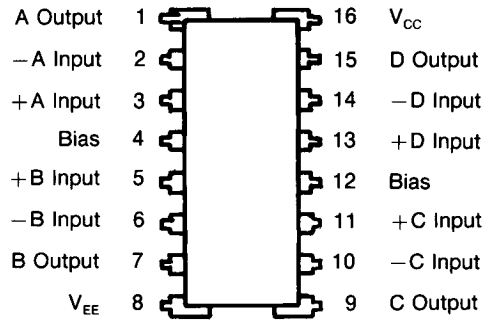


ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
	Difference between V_{CC} and V_{EE}	32	V
$V_{IN,DIFF}$	Differential Input Voltage	7	V
I_{Ref}	Reference Current	500	μA
I_{Out}	Output Current	20	mA
$T_{STORAGE}$		−55 to 125	°C
$T_{OPERATING}$		0 to 70	°C
P_D	Maximum Power Dissipation	375	mW
T_J	Maximum Junction Temperature	125	°C

*** Since this device does not have internal current limiting, the circuits being driven by pins 1, 7, 9 and 15 should have some form of current limiting to keep from exceeding the Absolute Maximum Rating (I_{OUT}) of 20 mA for this device.**

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS*	MIN	MAX	UNITS
V_{CC}	14.25	15.75	Volts
V_{EE}	−14.25	−15.75	Volts
Open Loop Voltage Amplification Condition: See Figure 1.	1000		
Input Offset Voltage Condition: R_L more than 100KΩ; Input connected to output; (+) Input grounded. Measure output voltage.		±5	mV
Risetime Condition: See Figure 2.		60	nS
Closed Loop Voltage Amplification Condition: See Figure 3.	9.70		
Output Voltage Swing Condition: Output voltage swing will not go more than 1.0 volt negative of (−) input.	±12.0		V
Noise Condition: Referred to Input.		100	μV/peak to peak

***The circuit conditions at which these parameter values were tested are:**
V_{CC} = +15 volts, V_{EE} = −15 volts; I_{REF} = 0.25 mA. All these values ±5.0%. T_A = 0 to +70°C.

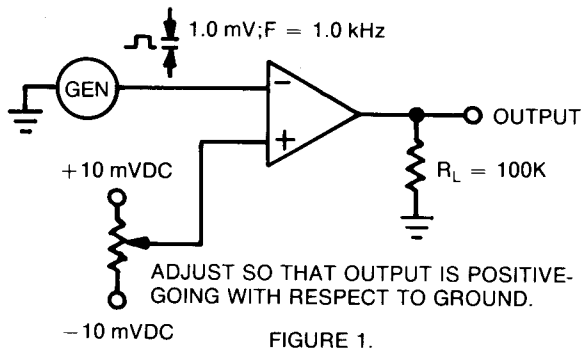


FIGURE 1.

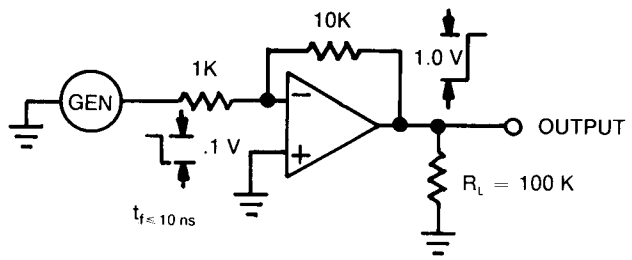


FIGURE 2.

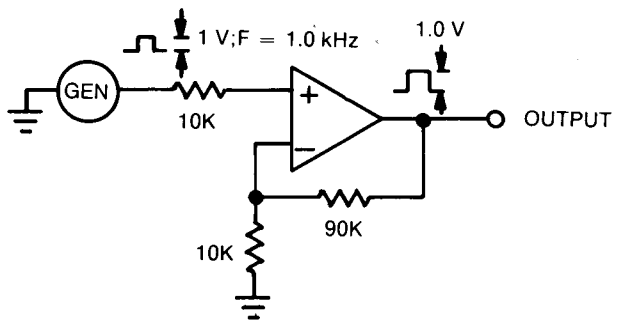
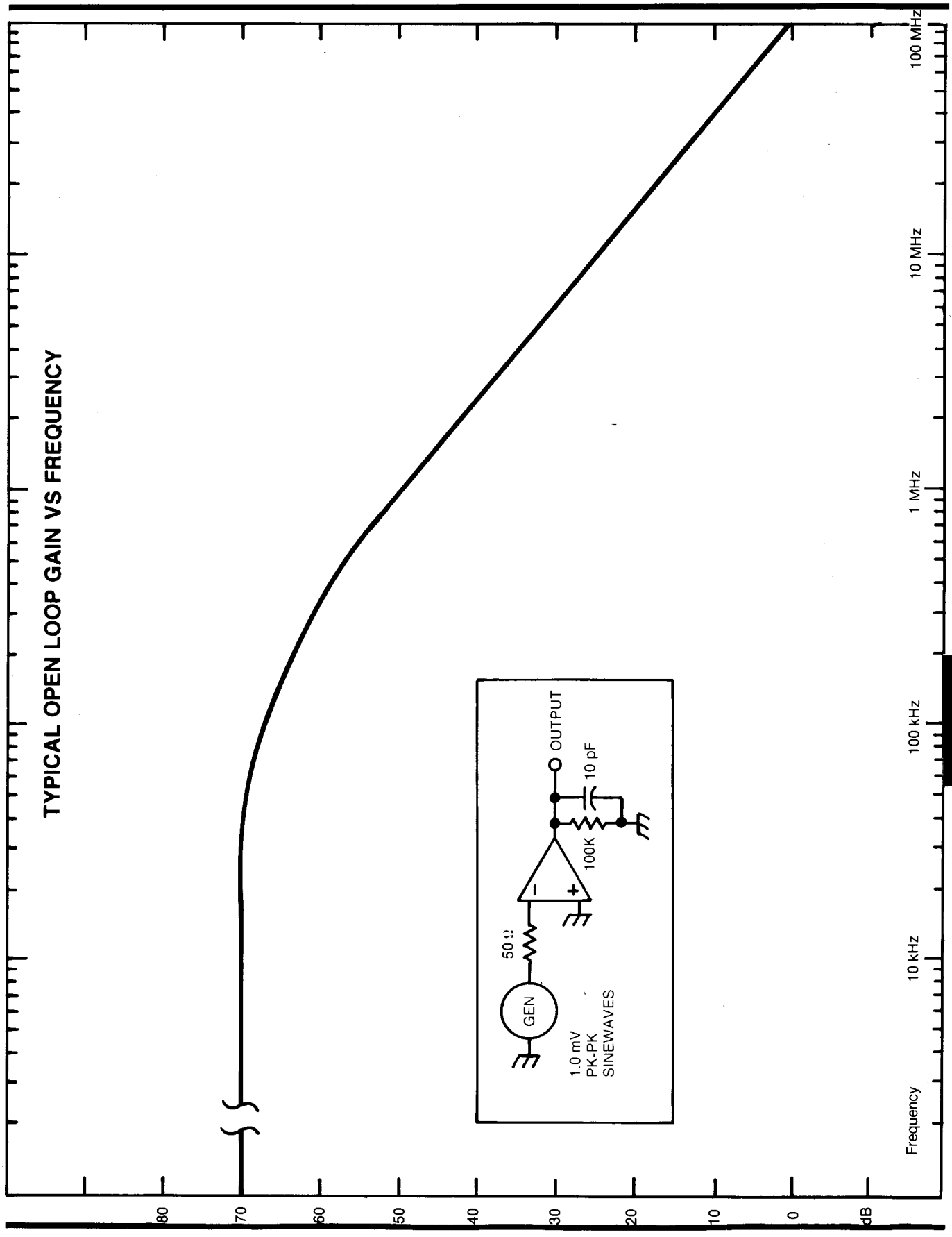


FIGURE 3


TYPICAL OPEN LOOP GAIN VS FREQUENCY
80
70
60
50
40
30
20
10
0
dB
Frequency
10 kHz
100 kHz
1 MHz
10 MHz
100 MHz
OUTPUT
10 pF
100K
50 Ω
GEN
1.0 mV
PK-PK
SINEWAVES

5

APPLICATIONS INFORMATION

RELIABILITY

λ, Failure Rate, .02%/1K hours at 75°C Tj
θ_{jc} = 94°C/W

D/A CONVERTER

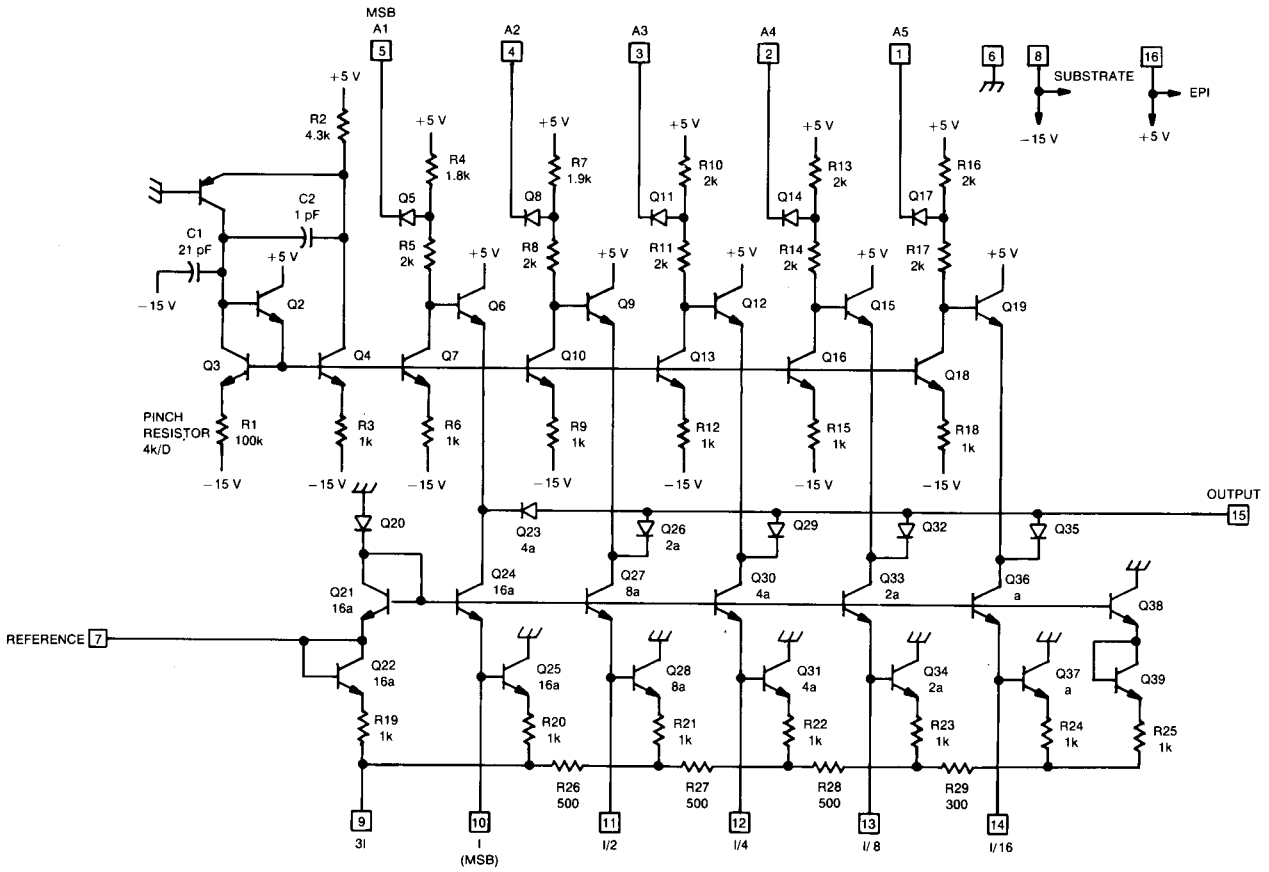
DESCRIPTION

The 155-0038-02 is a silicon monolithic digital-to-analog converter in a 16 lead dual-in-line hermetic package.

FEATURES

- 5-bit precision current source D/A converter.
- Current ratios set by external resistors.
- Range of MSB is 5 mA to 30 mA.
- Two packages may be used together for a 10-bit D/A with ±1/2 LSB accuracy.
- Output is designed to sum into 0 volts.
- Logic inputs are T^2L compatible with a low state being true.

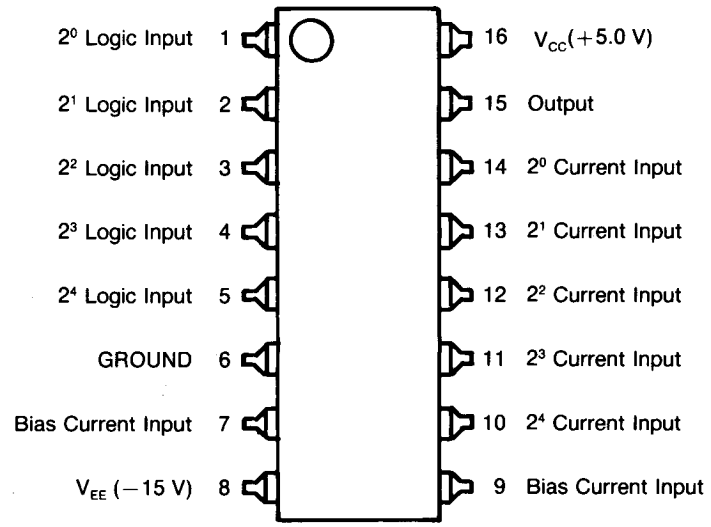
SCHEMATIC



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
T_{stg}	Storage Temperature	−55 to 125	°C
T_A	Operating Ambient Temperature	0 to 70	°C
V_{CC}	Positive Supply Voltage	10	V
V_{EE}	Negative Supply Voltage	−20	V

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

Electrical characteristics
(T_A = 0 to +70°C: V_{EE} = −15 V ±1.0%;
V_{CC} = +5.0 V ±1.0%; pin 9 current = 3 times
pin 10 current ±10%.

Symbols	Identifications	Notes and Test Conditions	Values Min	Max	Units
Pin 8	Negative-supply voltage		−5.0	−15.5	V
	Negative-supply current		4.5	7.6	mA
Pin 16	Positive-supply voltage		4.75	5.25	V
	Positive-supply current	All logic inputs HIGH	4.5	7.6	mA
		All logic inputs LOW	10	14	mA
Pins 1, 2, 3, 4, and 5	Logic input, voltage and current	Input HIGH	1.8	5.0	V
				1.0	μA
		Input LOW	0	0.7	V
				1.5	mA
Pin 11	Current-input voltage	See note 1	−0.5	+0.5	mV
Pin 12	Current-input voltage	See note 1	−1.0	+1.0	mV
Pin 13	Current-input voltage	See note 1	−2.0	+2.0	mV
Pin 14	Current-input voltage	See note 1	−4.0	+4.0	mV
	Current-input current		2.5		μA
Pin 10	Current-input current			5.0	mA
Pin 15	Output voltage		−100	+100	mV
	Output current	All inputs HIGH	0	1.0	μA
	Output-current accuracy	See note 2		0.032	%
Pin 15	Switching Speed	Delay time from the 50% point of a TTL input to the output within ±1/2 LSB of desired output.		50	nS

Note 1: Voltage with respect to pin 10.

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Note 2: Determine according to:

$$\text{Output-current accuracy, in percent} = \frac{\left(\frac{X}{31}\right)(I_{TOTAL} - I_{OUT})\,(100)}{\left(\frac{X}{31}\right)(I_{TOTAL})}$$

where X = step number (decimal equivalent of binary input),

I_{TOTAL} = current out with all logic inputs LOW,

I_{OUT} = current measured at pin 15 during selection of all possible combinations of pins 1 through 5.

Input-current conditions are:

I at pin 10

$\frac{I}{2}$ at pin 11

$\frac{I}{4}$ at pin 12

$\frac{I}{8}$ at pin 13

$\frac{I}{16}$ at pin 14

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RELIABILITY

λ, Failure rate, ≤0.02%/1K hours at 75°C Tj

TRIGGER SWEEP CIRCUIT

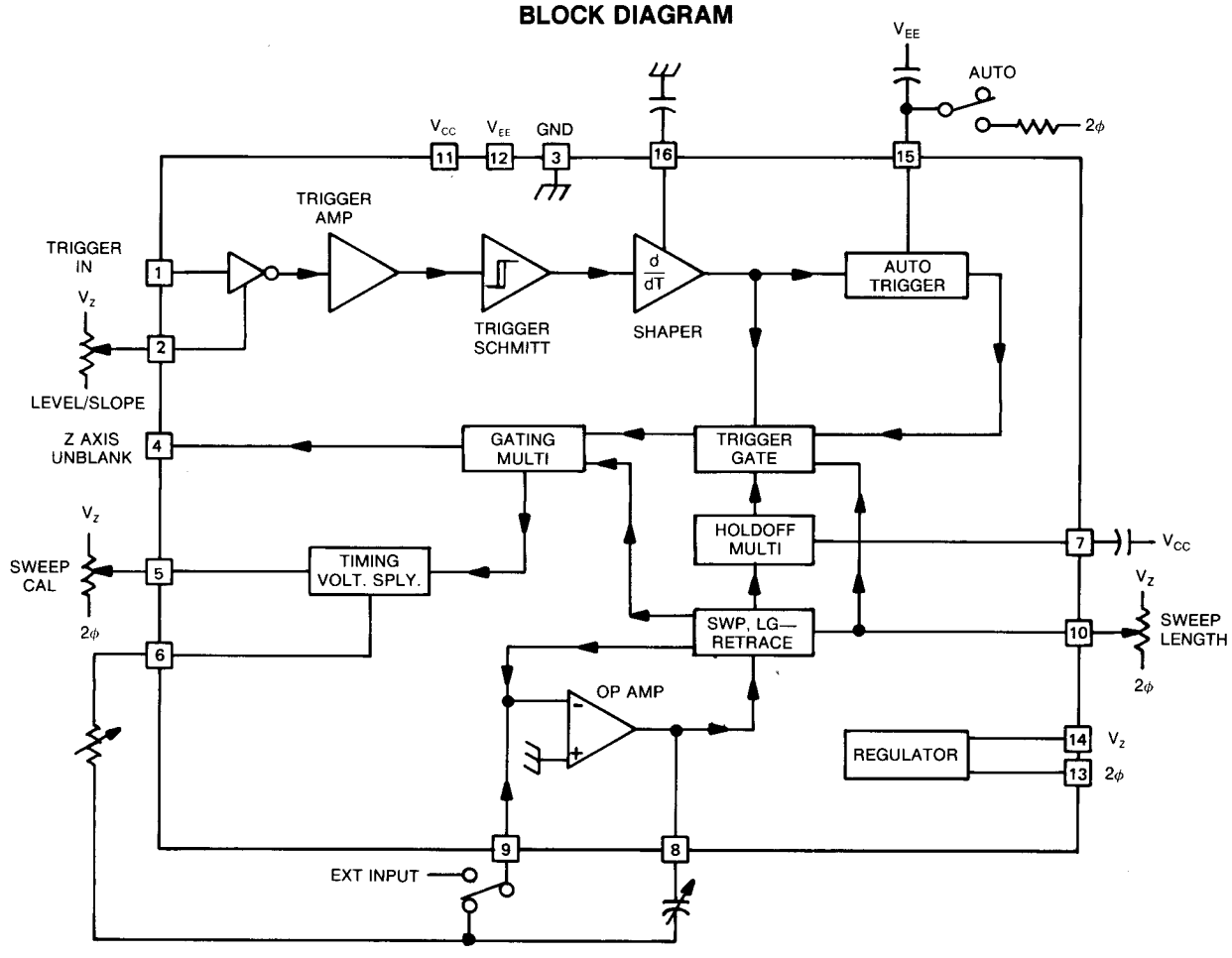
DESCRIPTION

The 155-0048-01 is a monolithic integrated circuit. This trigger sweep circuit is for use in low frequency (below 1 MHz) applications.

FEATURES

- Trigger slope/level selection
- Variable sweep rate and length with controlled timing supply
- High Z BIFET Miller and trigger inputs
- Sweep holdoff
- Auto trigger with adjustable holdoff
- Z-axis blanking
- Reference voltage outputs for stable sweep control
- External X-axis Input
- Available in 2 package styles minipak (155-0048-01) & DIP (155-0055-00)

BLOCK DIAGRAM



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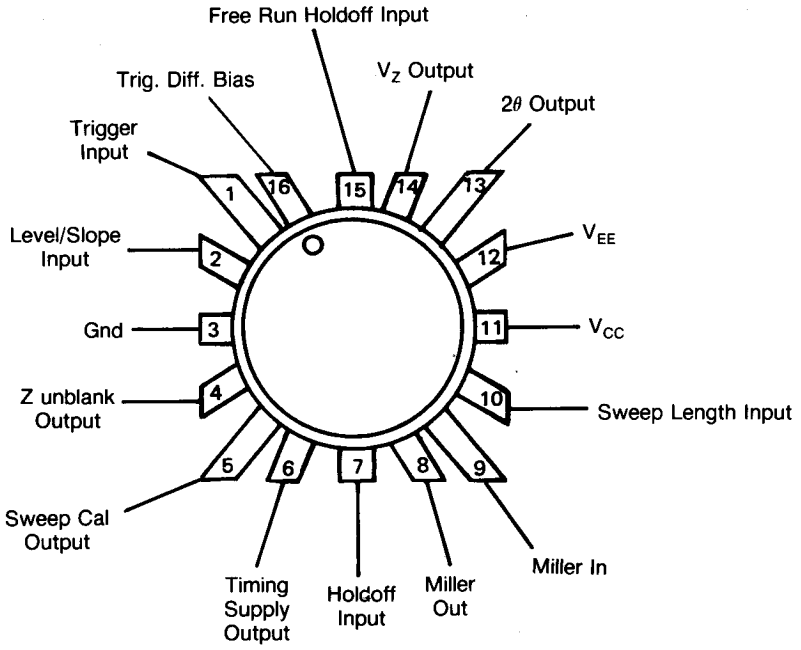
ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
V_{CC}	Maximum positive power supply voltage	+6.5	V
V_{EE}	Maximum negative power supply voltage	−6.5	V
	Trigger Input voltage	±4.6	V
V_Z	Current Load	4.75	mA
2θ	Current Load	4.75	mA
P_d	Power dissipation	300	mV
	Miller Out Source Current	2	mA
	Miller Out Sink Current	0.5	mA
	Voltage on input pins 2, 5, 10*		
$T_{STORAGE}$	Storage temperature range	−55 to +125	°C
$T_{OPERATING}$	Operating temperature range	−15 to +70	°C

*** Must not be less than 2θ or greater than Vz.**



ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS
V_{CC}	Positive Supply Voltage		5.0	6.5	V
V_{EE}	Negative Supply Voltage		−5.0	−6.5	V
I_{CC}	Positive Supply Current	V_{CC} = +6.5 V V_{EE} = −6.5 V Miller sweeping in auto mode		23	mA
I_{EE}	Negative Supply Current	Same as I_{CC}	−23		mA
V_{REF}	Internal Reference Voltage	Measure V_Z pin 14 Measure 2θ pin 13 $I_{VZ} = I_{2\theta}$ = 2.5 mA $V_{REF} = V_Z - 2\theta$	5.8	6.8	V
V_{OS}	Op amp input offset	Force op amp output pin 8 to 0 V Large (>1 MΩ) feedback resistor pin 8 to pin 9 Measure voltage on input pin 9	−.5	+.5	V
V_{OSTC}	Op amp input offset temperature coefficient	Same as V_{OS} over temperature	−.5	+.5	mV/°C
I_B	Op amp input bias current	Measure current into pin 9 from ground	0	5	nA
A_{OL}	Op amp open loop gain	DC signal on Pin 9 Measure pin 8 swing $A_{OL} = \frac{\Delta V_0 \text{ pin } 8}{\Delta V_1 \text{ pin } 9}$	80		
V_{OUT+}	+ peak of Miller output	Free run sweep Sweep length pin 10 = −2 V Measure + peak at pin 8	1.5	2.5	V
V_{OUT-}	− peak of Miller output	Same as V_{OUT+} Measure − peak at pin 8	−2.5	−1.5	V
I_{TL}	Timing supply sink current	Measure from pin 6 during sweep pin 5 = V_Z	−.5		mA
V_S	Trigger signal sensitivity	1 kHz square wave input ramped up in amplitude until sweep triggers	50		mV

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ELECTRICAL CHARACTERISTICS (cont)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS
F_{TS}	Maximum usable trigger frequency			1	MHz
I_{CFR}	Free run timing current	Measure pin 16 current in auto mode	35	65	μA
Z_T	Trigger input impedance		20	30	KΩ
I_{BT}	Trigger input bias current	Measure pin 1 current from ground	——	5	nA
T_V	Usable trigger input range	Ramp offset of 1 kHz, 50 mV square wave on Input pin 1 Measure offset at limits of triggering range	−875	+875	mA
I_{OLB}	Unblanking sink current	Measure pin 4 current during holdoff from V_{CC}	200	450	μA
V_{THL}	Timing voltage during holdoff	Voltage on 5 = 2θ Measure pin 6	−.5	+.5	V
V_{THH}	Timing voltage during holdoff	Voltage on pin 5 = V_Z	−4	−2	V
V_{TRL}	Timing voltage during sweep	Voltage on pin 5 = 2θ	−.5	+.5	V
V_{TRH}	Timing voltage during sweep	Voltage on pin 5 = V_Z	2.5	3.5	V
I_{TH}	Timing supply source current	Measure from pin 6 during holdoff pin 5 = V_Z	——	1	mA

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APPLICATIONS INFORMATION

Applications

The internal reference voltage output should be used as sources on control networks for sweep cal, sweep length, and level/slope. These sources will track internal bias shifts over temperature.

When sweep length input is forced higher than 7.2 volts above V_{EE}, trigger is disabled to gating multi and op amp may be used as external X axis amplifier with Z axis unblanked.

When the auto holdoff timing pin is pulled low, the auto trigger is disabled.

When the holdoff timing pin is held high, the trigger to gating multi is disabled and sweep is "held off".

Typical holdoff capacitor valve is one-tenth of C_{TIMING}.

Some low frequency applications may experience a timing supply oscillation which can be squelched with a 390 Ω, 87 pF RC series network connected to Miller/op amp output.

Typical temperature coefficient of $V_Z - 2\theta$ is .03%/°C.

Differentiator capacitor on Pin 11 should be 27 to 100 pF.

Product Precautions

Input Protection

Pins 1 and 9 (BIFET gates) applied voltage should be between −4.6 and +4.6 V.

Pins 2, 5, and 10 applied voltage should be between V_{EE} and V_{CC}.

Output Loading

Voltage on pin 4 should be kept 15 V above 2 θ.

V_Z and 2 θ outputs should be loaded 4.75 mA each.

Pin 8 loading should be kept 2 mA source and 0.5 mA sink.

Power Supply Turn-On/Turn-Off Sequence

Power on sequence:

First: V_{ee} (−6 V)

Second: V_{cc} (+6 V)

Handling Procedures

Standard Mini-Pak mounting techniques should be employed. Removal from socket should be accomplished with force applied to the plastic body rather than the leads.

Parts should be handled and transported with materials approved to dissipate static charges and keep the device leads equipotential.

RELIABILITY

λ, Failure rate .02%/1k hours at 75°C T.

θ_{jc} = 97.7°C/W

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SWEEP CONTROL

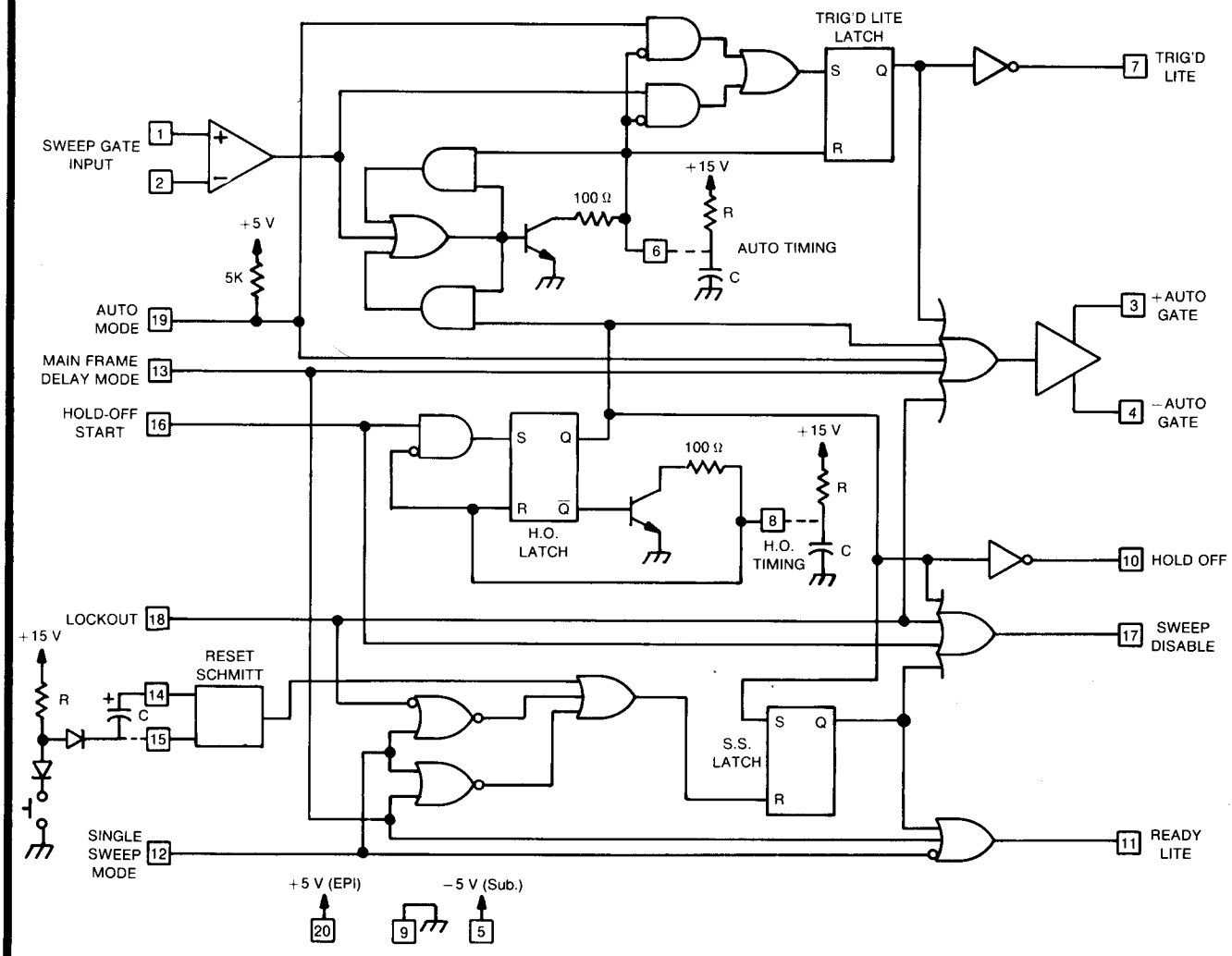
DESCRIPTION

The sweep control IC contains bright baseline Auto, Single Sweep, and Holdoff logic. Lamp drivers are provided for Single Sweep and Trigger Lights. It also contains Lockout and Main Frame delay mode controls used in 7000 Series Scopes.

FEATURES

- Sweep gate input, 0.125 V differential signal generates a triggered gate.
- Auto bright baseline time constant determined by external R-C.
- Holdoff time constant determined by external R-C.
- Single sweep mode.
- Auto gate outputs.
- 60 mA drive for trigger and reset light bulbs.

LOGIC DIAGRAM



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	MIN	MAX	UNITS
T-A	Operating Ambient Temperature	−15°C	+75°	C
T-J	Junction Temperature T-A = 75°C Power = 250 mW		+99°	C
T-STG	Storage Temperature	−55°	+125°	C
V_{CC}	Positive Supply	+4.00	+6.00	V
V_{EE}	Negative Supply	−4.00	−6.00	V
I_C	Sink Current into Lamp Drivers (Pins 7 and 11)		100	mA
I_C	Sink Current into Hold-Off Out (Pin 10)		10	mA

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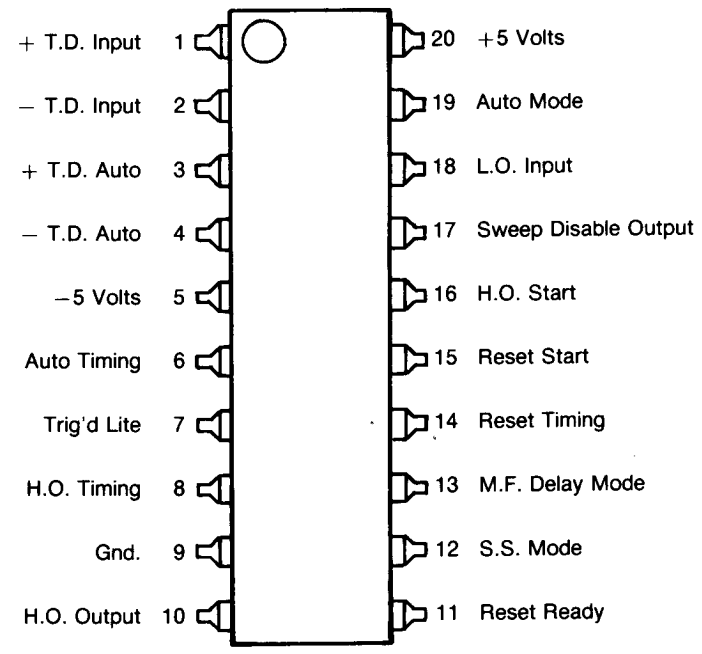
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PIN(S)	SYMBOL	NAME	MIN	MAX	UNITS
1&2	DR	DYNAMIC RANGE	−500	500	mV
1&2	I_{LEAK}	INPUT LEAKAGE		50	μA
3	$\overline{I_{OUT}}$	OUTPUT CURRENT (Absence of Gate)		100	μA
3	I_{OUT}	OUTPUT CURRENT (Presence of Gate)	2.7	3.7	mA
4	I_{OUT}	OUTPUT CURRENT (Presence of Gate)		100	μA
4	$\overline{I_{OUT}}$	OUTPUT CURRENT (Absence of Gate)	2.7	3.7	mA
3&4	V_{OUT}	VOLTAGE TO GND	−0.5	5.50	V
5	V_{EE}	NEGATIVE SUPPLY VOLTAGE	−4.8	−5.2	V
5	I_{EE}	−5 VOLT SUPPLY CURRENT	15	35	mA
6	R_{IN}	INPUT IMPEDANCE (while charging)	500		kΩ
8	R_{IN}	INPUT IMPEDANCE (while charging)	1.0		MΩ
6&8	I_{LEAK}	INPUT LEAKAGE (while charging)		10	μA
6&8	$V_{DIS.}$	DISCHARGED VOLTAGE I_C = 1.5 mA		360	mV
7&11	V_{SAT}	TRANSISTOR SATURATION I_C = 60 mA		700	mV
7&11	I_{LEAK}	OFF CURRENT V_C = 5 VOLTS		40	μA
10	$V_{SAT.}$	TRANSISTOR SATURATION I_C = 5 mA		400	mV
10	I_{LEAK}	OFF CURRENT V_C = 5 VOLTS		10	μA
12	V_{IN}	S.S. MODE HI VOLTAGE IN, R_{IN} = 800 Ω MIN.	4.0	5.5	V

ELECTRICAL CHARACTERISTICS (cont)

PIN(S)	SYMBOL	NAME	MIN	MAX	UNITS
12	$\overline{V_{IN}}$	S.S. MODE LO VOLTAGE IN R_{IN} = 5 KΩ MIN.	−300	300	mV
13	V_{IN}	M.F. DELAY MODE HI VOLTAGE IN R_{IN} = 1.5 KΩ MIN.	4.0	5.5	V
13	$\overline{V_{IN}}$	M.F. DELAY MODE LO VOLTAGE IN R_{IN} = 1 MΩ MIN.	−300	300	mV
16	V_{IN}	H.O. START HI VOLTAGE IN R_{IN} = 2 KΩ MIN.	2.2	2.8	V
16	$\overline{V_{IN}}$	H.O. START LO VOLTAGE IN R_{IN} = 1 MΩ MIN.	−300	300	mV
17	V_{OUT}	SWEEP DISABLE HI Nominal Current = 5 mA	1.55		V
17	$\overline{V_{OUT}}$	SWEEP DISABLE LO	−1.10	−0.45	V
18	V_{IN}	LOCKOUT HI VOLTAGE IN R_{IN} = 1 KΩ MIN.	2.5	5.5	V
18	$\overline{V_{IN}}$	LOCKOUT LO VOLTAGE IN R_{IN} = 1 KΩ MIN.	−300	300	mV
20	V_{CC}	POSITIVE SUPPLY VOLTAGE	4.8	5.2	V
20	I_{CC}	+5 VOLTS SUPPLY CURRENT	12	16	mA

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APPLICATIONS INFORMATION

Input Features

Sweep Gate Input Pins 1&2—A differential signal of ±0.125 V from ground will cause the input emitter coupled pair to switch and generate a triggered gate inside the IC.

Auto Timing Pin 6—Refer to Figure 1. The auto bright baseline time constant is determined by an external R-C connected to pin 6 as shown. The switching point needed to determine the R-C is +4.2 V ±.3 V. When the timing reset has been initiated with a trigger, the voltage at pin 6 must recover to less than +1 volt before recharging can begin.

Hold-Off Timing Pin 8—Refer to Figure 2. The hold-off time constant is determined by an external R-C as shown. The switching point occurs at +4.2 ± .3 V.

Single Sweep Mode Pin 12—A nominal +5 volt signal applied to pin 12 places the IC in single sweep mode and allows reset ready lite to be on when the reset button is pushed (pin 15). Open circuit or grounding of pin 12 places the IC in auto or normal triggering mode.

Main Frame Delay Mode Pin 13—A nominal +5 volt signal applied to pin 13 sets the IC to single sweep mode but does not allow lighting of reset ready lite. High also inhibits the auto circuit. Reset to Ready is accomplished with the rise of LOCKOUT (pin 18).

Reset Timing and Reset Start Pins 14 & 15—Refer to Figures 3 and 4. A closure of RESET to ground will generate a reset pulse causing the single sweep latch to be reset and lighting the RESET READY LITE (pin 11).

Hold-Off Start Pin 16—This is the input pin to reset the sweep and initiate holdoff. The incoming waveform is intended to be short with respect to sweep duration as might be supplied from a sweep end comparator. High is +2.5 volts min.

Lockout Pin 18—A minimum of +2.5 volts applied to pin 18 will cause SWEEP DISABLE (pin 17) to go high and will reset the single sweep latch if in main frame delaying mode. LOCKOUT will not reset the single sweep latch in single sweep mode.

Auto Mode Pin 19—This pin is to be grounded for bright baseline auto operation. When pin 19 is grounded and no triggers have been present (pin 1 negative with respect to pin 2) for more than the time constant set at pin 6, then the auto gate occurs at pins 3 and 4.

Auto Gate Outputs Pins 3 & 4—The occurance of an auto gate will cause the differential switching of a nominal 3.2 mA of current from pin 4 to pin 3.

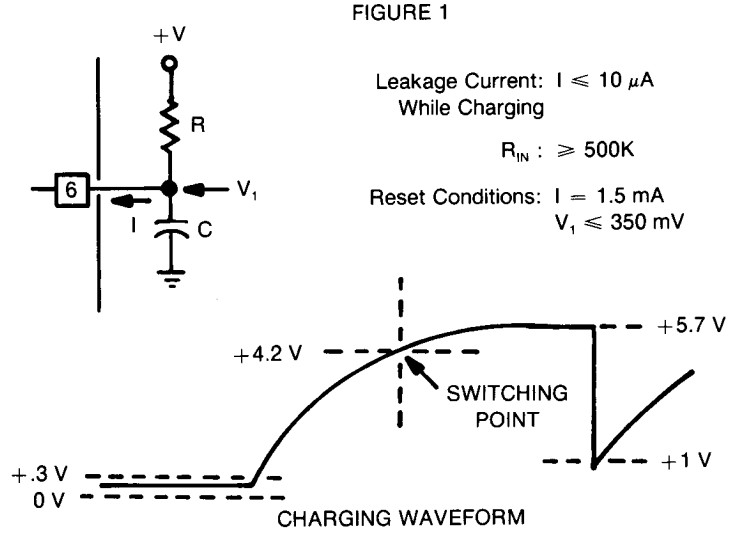
Trigger Lite Pin 7—This pin is pulled to ground to sink 60 mA of lamp current when a trigger gate has occurred.

Hold-Off Pin 10—This is a current sink to ground during hold-off. Maximum sink current is 5 mA.

Reset Ready Lite Pin 11—This pin is pulled to ground to sink 60 mA of lamp current when a high is supplied to pin 12 and no triggers are present (S.S. latch reset and pin 13 low).

Sweep Disable Out Pin 17—This signal is used to reset and holdoff the sweep. A high at this pin will reset the sweep if it is running and the sweep will be held off as long as it is high.

FIGURE 1

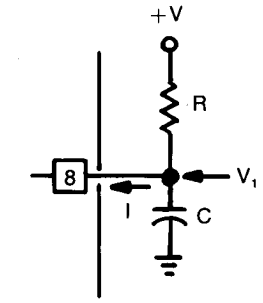


Leakage Current: $I \leq 10\ \mu A$
While Charging

R_{IN} : $\geq$ 500K

Reset Conditions: $I = 1.5$ mA
$V_1 \leq 350$ mV

FIGURE 2



Leakage Current: $I \leq 10\ \mu A$
While Charging

R_{IN} : $\geq$ 1 Meg.

Reset Conditions: $I = 1.5$ mA
$V_1 \leq 350$ mV

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FIGURE 3

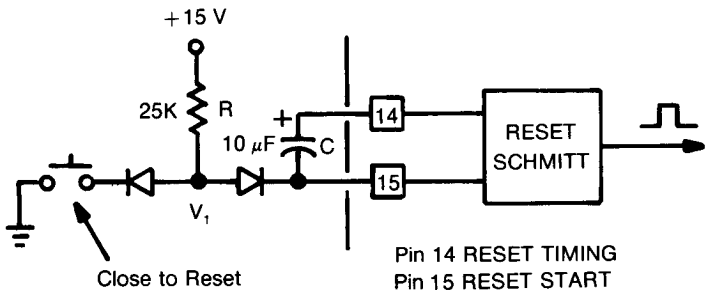
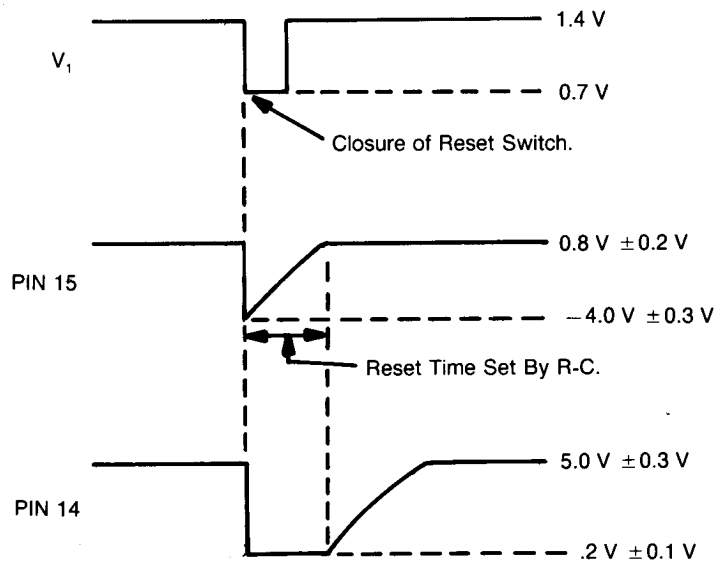


FIGURE 4



RELIABILITY

λ, Failure Rate ≤ .02%/1K hours at 75°C Tj

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TRIGGER SWEEP CIRCUIT

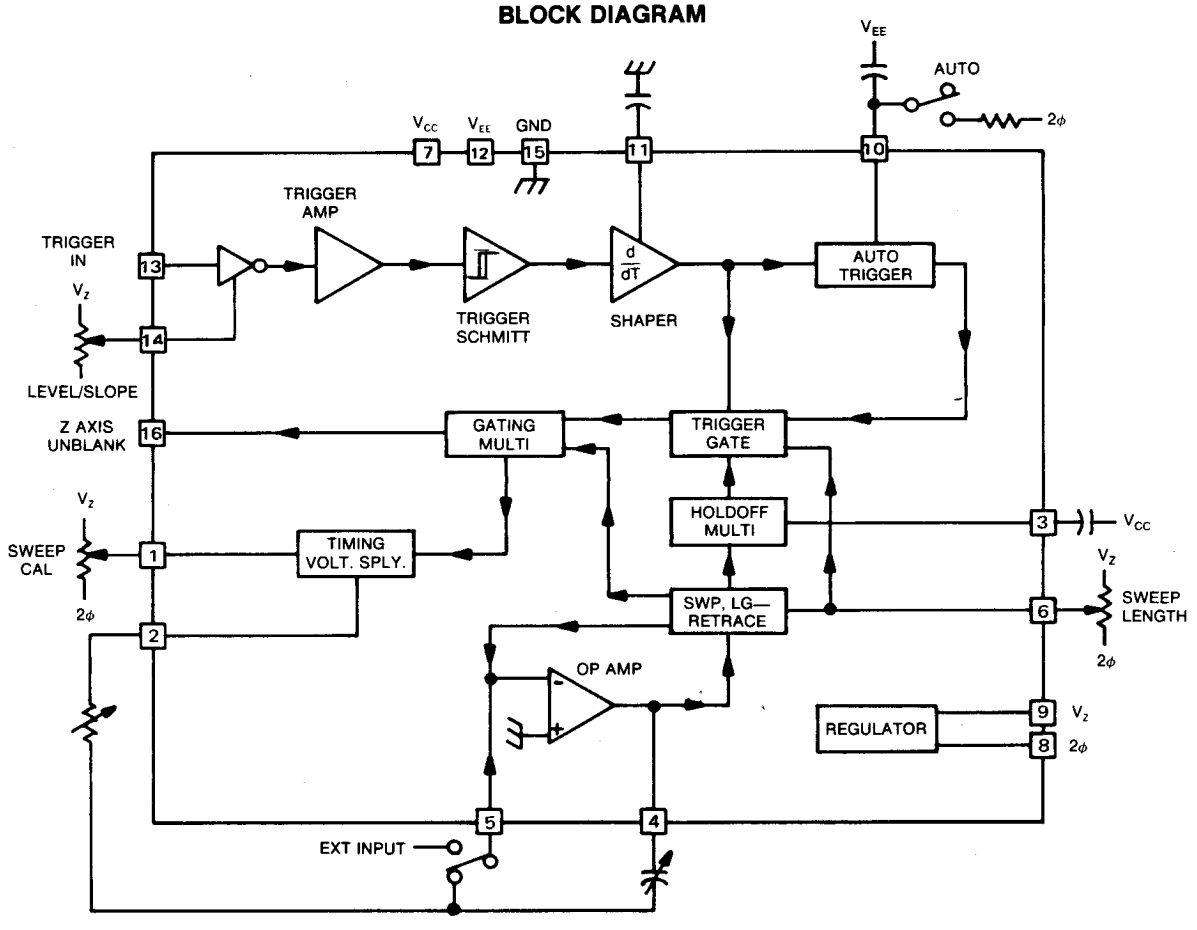
DESCRIPTION

The 155-0055-00 is a monolithic integrated circuit. This trigger sweep circuit is for use in low frequency (below 1 MHz) applications.

FEATURES

- Trigger slope/level selection
- Variable sweep rate and length with controlled timing supply
- High Z BIFET Miller and trigger inputs
- Sweep holdoff
- Auto trigger with adjustable holdoff
- Z-axis blanking
- Reference voltage outputs for stable sweep control
- External X-axis Input
- Available in 2 package styles
  minipak (155-0048-01) & DIP (155-0055-00)

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
V_{CC}	Maximum positive power supply voltage	+6.5	V
V_{EE}	Maximum negative power supply voltage	−6.5	V
	Trigger Input voltage	±4.6	V
V_Z	Current Load	4.75	mA
2θ	Current Load	4.75	mA
P_d	Power dissipation	300	mV
	Miller Out Source Current	2	mA
	Miller Out Sink Current	0.5	mA
	Voltage on input pins 2, 5, 10*		
$T_{STORAGE}$	Storage temperature range	−55 to +125	°C
$T_{OPERATING}$	Operating temperature range	−15 to +70	°C

*** Must not be less than 2θ or greater than Vz.**

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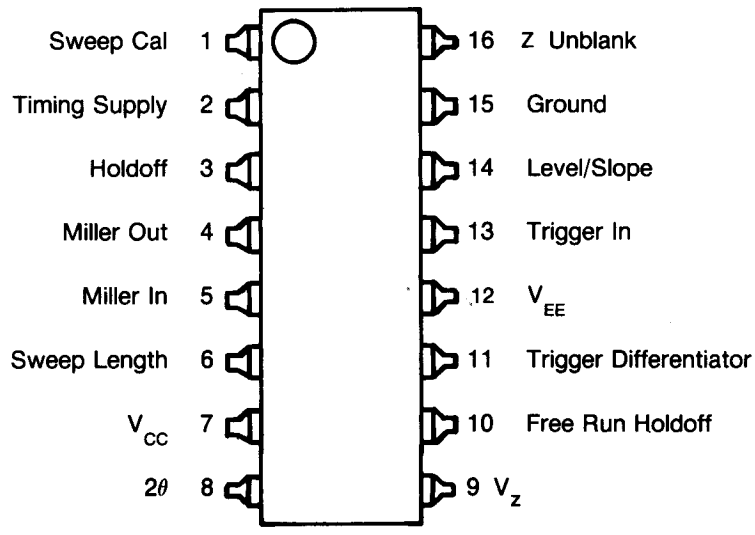
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS
V_{CC}	Positive Supply Voltage		5.0	6.5	V
V_{EE}	Negative Supply Voltage		−5.0	−6.5	V
I_{CC}	Positive Supply Current	V_{CC} = +6.5 V V_{EE} = −6.5 V Miller sweeping in auto mode		23	mA
I_{EE}	Negative Supply Current	Same as I_{CC}	−23		mA
V_{REF}	Internal Reference Voltage	Measure V_Z pin 14 Measure 2θ pin 13 $I_{VZ} = I_{2\theta}$ = 2.5 mA $V_{REF} = V_Z - 2\theta$	5.8	6.8	V
V_{OS}	Op amp input offset	Force op amp output pin 8 to 0 V Large (>1 MΩ) feedback resistor pin 8 to pin 9 Measure voltage on input pin 9	−.5	+.5	V
V_{OSTC}	Op amp input offset temperature coefficient	Same as V_{OS} over temperature	−.5	+.5	mV/°C
I_B	Op amp input bias current	Measure current into pin 9 from ground	0	5	nA
A_{OL}	Op amp open loop gain	DC signal on Pin 9 Measure pin 8 swing $A_{OL} = \frac{\Delta V_0 \text{ pin } 8}{\Delta V_1 \text{ pin } 9}$	80		
V_{OUT+}	+ peak of Miller output	Free run sweep Sweep length pin 10 = −2 V Measure + peak at pin 8	1.5	2.5	V
V_{OUT-}	− peak of Miller output	Same as V_{OUT+} . Measure − peak at pin 8	−2.5	−1.5	V
I_{TL}	Timing supply sink current	Measure from pin 6 during sweep pin 5 = V_Z	−.5		mA
V_S	Trigger signal sensitivity	1 kHz square wave input ramped up in amplitude until sweep triggers	50		mV

5

ELECTRICAL CHARACTERISTICS (cont)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS
F_{TS}	Maximum usable trigger frequency			1	MHz
I_{CFR}	Free run timing current	Measure pin 16 current in auto mode	35	65	μA
Z_T	Trigger input impedance		20	30	KΩ
I_{BT}	Trigger input bias current	Measure pin 1 current from ground	——	5	nA
T_V	Usable trigger input range	Ramp offset of 1 kHz, 50 mV square wave on Input pin 1 Measure offset at limits of triggering range	−875	+875	mA
I_{OLB}	Unblanking sink current	Measure pin 4 current during holdoff from V_{CC}	200	450	μA
V_{THL}	Timing voltage during holdoff	Voltage on 5 = 2θ Measure pin 6	−.5	+.5	V
V_{THH}	Timing voltage during holdoff	Voltage on pin 5 = V_Z	−4	−2	V
V_{TRL}	Timing voltage during sweep	Voltage on pin 5 = 2θ	−.5	+.5	V
V_{TRH}	Timing voltage during sweep	Voltage on pin 5 = V_Z	2.5	3.5	V
I_{TH}	Timing supply source current	Measure from pin 6 during holdoff pin 5 = V_Z	——	1	mA

5

APPLICATIONS INFORMATION

Applications

The internal reference voltage output should be used as sources on control networks for sweep cal, sweep length, and level/slope. These sources will track internal bias shifts over temperature.

When sweep length input is forced higher than 7.2 volts above V_{EE}, trigger is disabled to gating multi and op amp may be used as external X axis amplifier with Z axis unblanked.

When the auto holdoff timing pin is pulled low, the auto trigger is disabled.

When the holdoff timing pin is held high, the trigger to gating multi is disabled and sweep is "held off".

Typical holdoff capacitor valve is one-tenth of C_{TIMING}.

Some low frequency applications may experience a timing supply oscillation which can be squelched with a 390 Ω, 87 pF RC series network connected to Miller/op amp output.

Typical temperature coefficient of $V_Z - 2\theta$ is .03%/°C.

Differentiator capacitor on Pin 11 should be 27 to 100 pF.

Product Precautions

Input Protection

Pins 1 and 9 (BIFET gates) applied voltage should be between −4.6 and +4.6 V.

Pins 2, 5, and 10 applied voltage should be between V_{EE} and V_{CC}.

Output Loading

Voltage on pin 4 should be kept 15 V above 2 θ.

V_Z and 2 θ outputs should be loaded 4.75 mA each.

Pin 8 loading should be kept 2 mA source and 0.5 mA sink.

Power Supply Turn-On/Turn-Off Sequence

Power on sequence:

First: V_{ee} (−6 V)

Second: V_{cc} (+6 V)

Handling Procedures

Standard Mini-Pak mounting techniques should be employed. Removal from socket should be accomplished with force applied to the plastic body rather than the leads.

Parts should be handled and transported with materials approved to dissipate static charges and keep the device leads equipotential.

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RELIABILITY

λ, Failure rate .02%/1k hours at 75°C T.

θ_{jc} = 97.7°C/W

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DUAL OP. AMP./CURRENT SOURCES

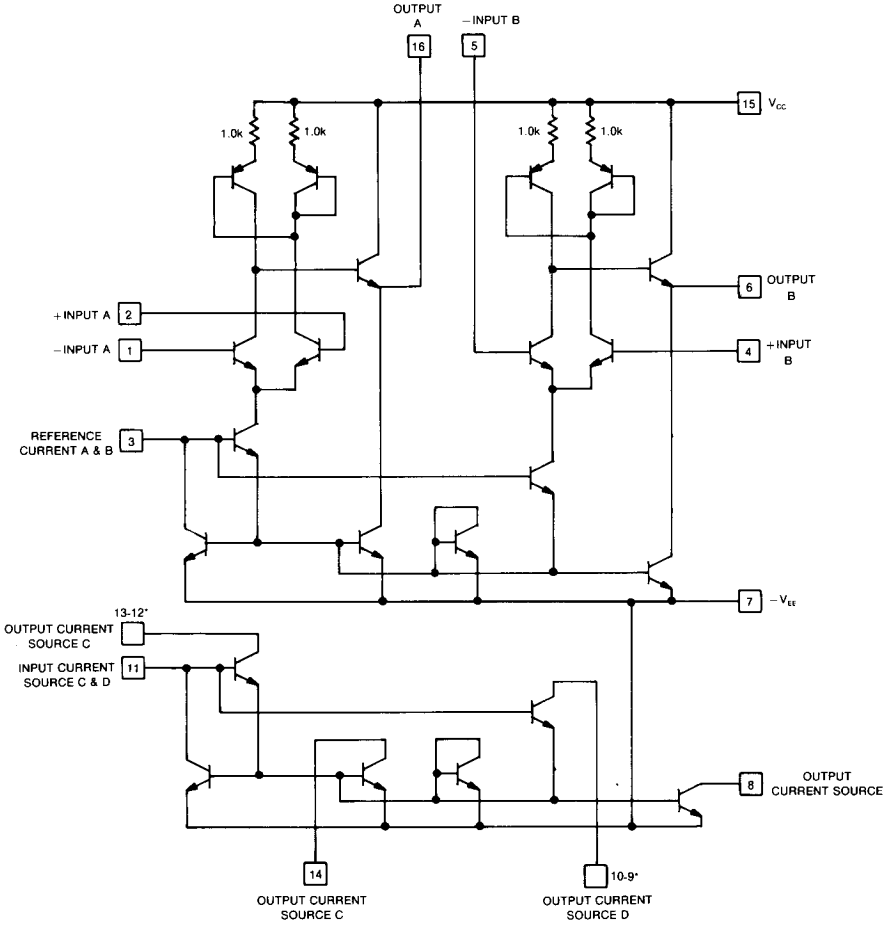
DESCRIPTION

The 155-0057-00 is a dual-operational amplifier with two current sources. The monolithic chip is contained in a 16-pin plastic package.

FEATURES

- ±5 V to ±15 V power supply range
- 80 MHz gain bandwidth product
- No compensation required
- Open loop gain 3300 typical
- 5 mV input offset voltage
- 5 mA output current

SCHEMATIC



*These two pins must be connected together externally.

5

ABSOLUTE MAXIMUMS

Symbols	Identifications	Values	Units
T_{stg}	Storage temperature, range	−55 to +125	°C
T_A	Operating ambient temperature, range	−15 to +60	°C
V_{CC} - V_{EE}	Difference between V_{CC} and V_{EE}	20	V
I_{out}	Output current (pins 16, 6)	5	mA
$V_{in,diff}$	Input differential voltage	±7.0	V
I_{REF}	Reference Current (pin 3)	500	μA
I_s out	Current Source Output (pins 8, 9, 10 or 12, 13, 14)	3	mA
I_s in	Current Source Input (pin 11)	1.5	mA
I_Z	Current Source Output Impedance	⩾200	KΩ
I_{volts}	Voltage Swing of Current Source Output	V_{EE} + 1.5 V to V_{EE} +20 V	V

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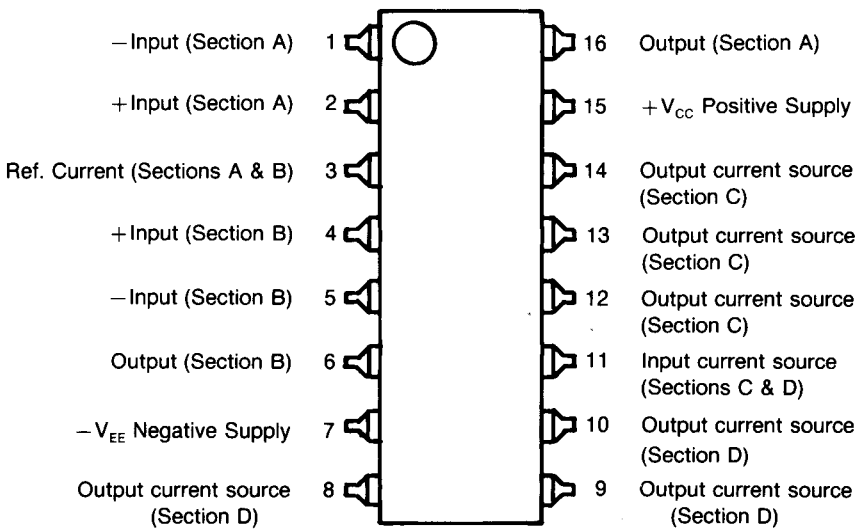
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

Electrical Characteristics (T_A = −15 to +60°C; V_{CC} = +6.5 V V_{EE} = −6.5 V; I_{REF} = 0.25 mA—Sections A & B ±1.0 percent Test each of 2 circuits.)
I_S In = .75 mA ±1.0%. Test both current sources.

Symbols	Identifications	Notes and Test Conditions	Values			
			Min	Typ	Max	Units
	Stability (Sections A & B)	−INPUT connected to OUTPUT; +INPUT to GROUND	No motorboating, oscillation, or other instability indication			
A_o	Open-loop voltage amplification (Sections A & B)	See Figure 1	1,000		3,300	
V_{os}	Section A Input offset voltage Section B	R_L >100 KΩ; −INPUT connected to OUTPUT; +INPUT grounded. Measure OUTPUT voltage			±5 ±10	mV
t_r	Risetime (Sections A & B)	See Figure 3			100	ns
A_c	Closed-loop voltage amplification (Sections A & B)	See Figure 4	9.70			
I_sOut	Output current from current sources. (Sections C & D)	See Figure 5	2.75	3.0	3.25	mA
	Output-voltage swing (Sections A & B)	−INPUT connected to OUTPUT; +INPUT connected to adjustable ±6.5 V supply. See Note 2	±4.0			V
	Frequency response (Sections A & B)	See Figure 2				
	Noise (Sections A & B)	Referred to input		10	100	μV peak-to-peak

[1]Test-condition tolerances, ±1.0 percent unless shown otherwise.

[2]OUTPUT voltage will not go more than 1.0 volt negative of −INPUT.

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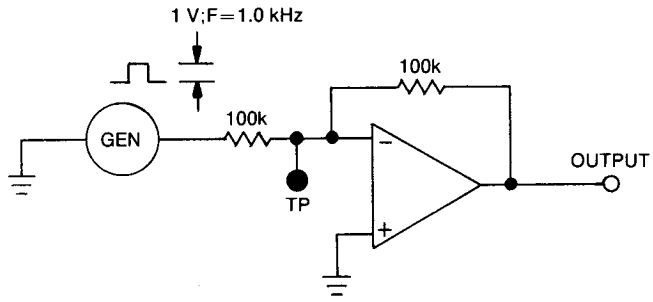

FIGURE 1

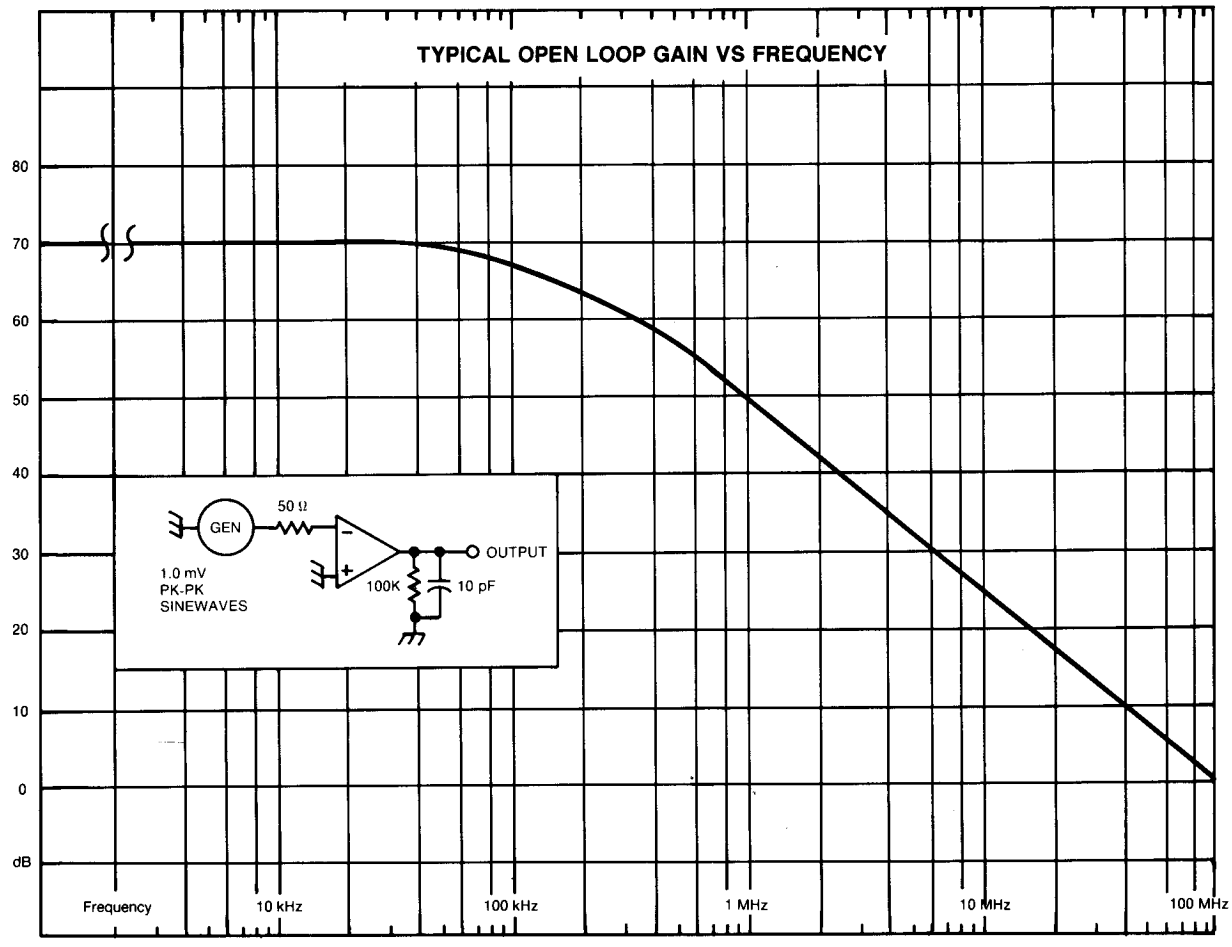

FIGURE 2

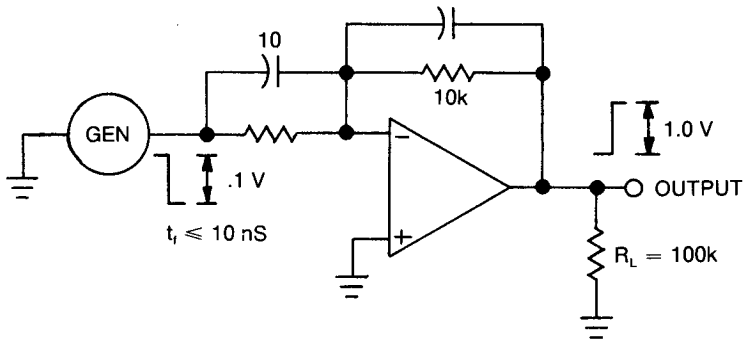

FIGURE 3

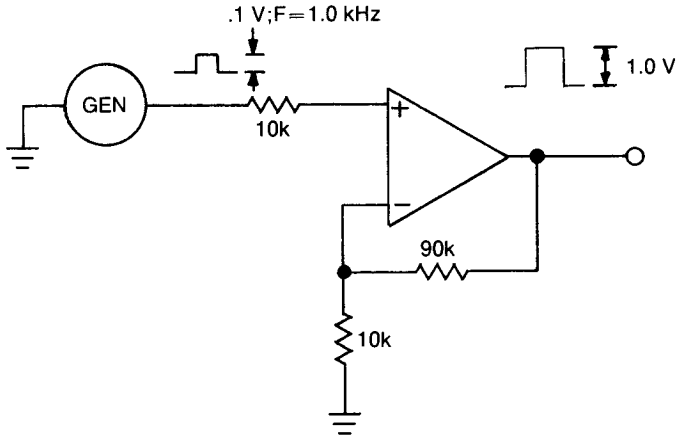

FIGURE 4

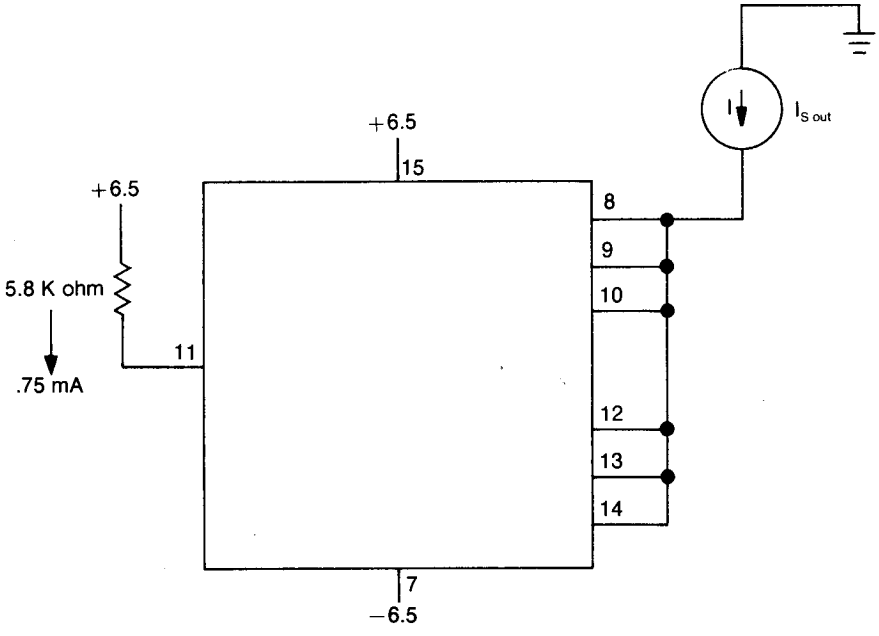

FIGURE 5

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DC-TO-DC CONTROLLER

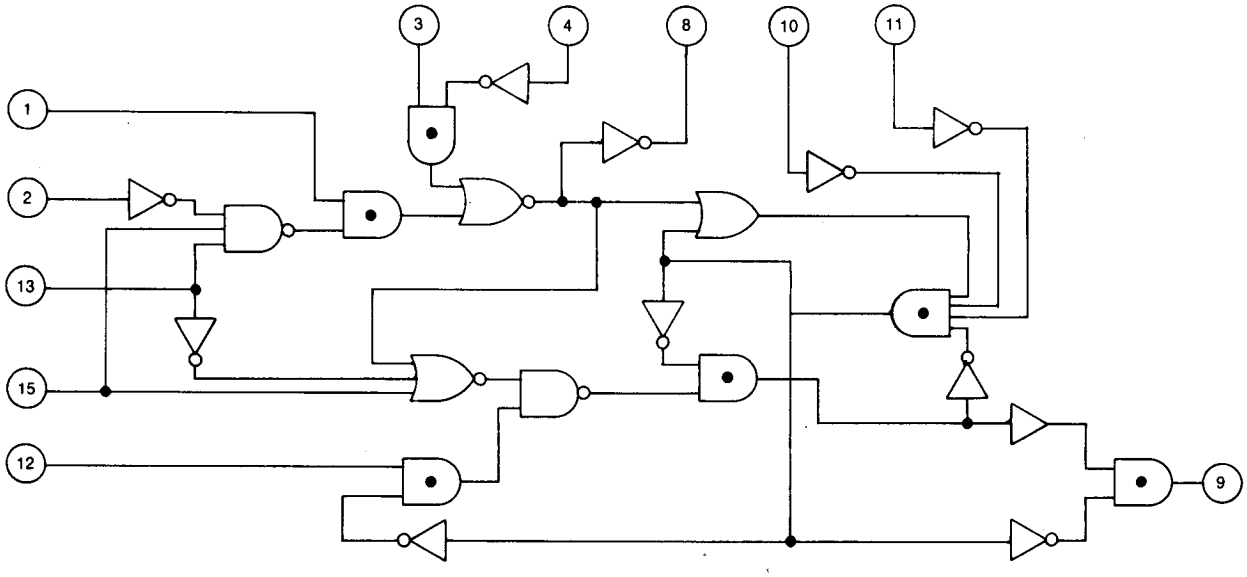
DESCRIPTION

The 155-0067-02 is a DC to DC controller for inverter power supplies. It provides circuitry to do all regulation and protection of the inverter system.

Inputs provided to:

- Sense and control secondary voltage faults
- Sense and limit the maximum inverter current
- Sense line voltage fluctuations
- Sense inverter current phase

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

Electrical

MAX RATING

Pin 1	−6.0 to + 2.0	V
Pin 2	−6.0 to + 0.5	V
Pin 3	−6.0 to + 2.0	V
Pin 4	−6.0 to + 2.0	V
Pin 5	——— GROUND ———	
Pin 6 NEVER APPLY VOLTAGE TO THIS PIN	8 to 30	mA
Pin 7	−15.0 to + 6.0	V
Pin 8	0 to + 10.0	V
Pin 9	0 to + 5.0	V
Pins 10 & 11	±2	mA
Pin 12	0 to + 2.5	V
Pin 13	−6.0 to + 6.0	V
Pin 14	−0.6 to + 0.6	V
Pin 15	−0.6 to + 1.0	V
Pin 16	——— GROUND ———	

Environmental

Operating Temperature Range	−20°C to +75°C
Storage Temperature Range	−55°C to +125°C

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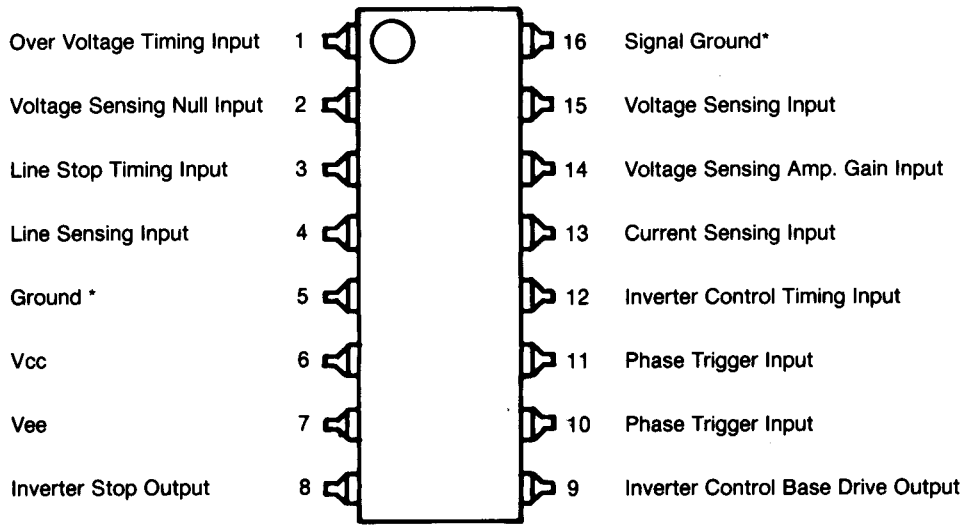
PIN CONNECTIONS



*Short together outside of package.

ELECTRICAL CHARACTERISTICS

Pin #	Parameter	Conditions	Limits		Units
			Min	Max	
1	Over voltage timing	Logic "0" at I1 = .1 mA Logic "1"	0.02	0.30	V
2	Voltage sense null (Fault)	Threshold (neg.) (pos.) If pin 2 > Vth, then V1 = logic "1" Input bias current: V2 > |210 mV| V2 > |150 mV|	−210 +150 −25 −1.0	−150 +210 +25 +1.0	 μA μA
3	Stop timing	Logic "0" at 13 = 2 mA Logic "1"	0.02 0.85	0.49 1.10	V V
4	Line sensing (stop delay)	Logic "0" Logic "1" Input bias current: V4 = 0.85 V	0.02 0.85 0.0	0.30 1.10 500	V V μA
5	GROUND	Connect to pin 16 external to package			
6	Vcc (internal)	Drive with an external current source from 9.0 mA to 30.0 mA	7.15	7.75	V
7	Vee (substrate)	Applied voltage Iee at V7 = −2.0 V	−3.0 1.8	−1.8 4.0	V mA
8	Inverter stop	Logic "0" at 18 = 2 mA Logic "1"	0.02 0.85	0.30 10.0	V V
9	Inverter control	0.5 V source to pin 9 Logic "0" (sinking) Logic "1" (sourcing)	 4.0 −12.0	 8.0 −4.0	mA mA
10/11	Phase triggers	In = −1 mA (logic "0") In = +1 mA (logic "1")	−0.85 0.02	0.02 0.85	V V
12	Inverter control timing	Logic "0" at 112 = 1.5 mA Logic "1"	0.15 0.85	0.48 10.0	V V
13	Current sense	Logic "0" Logic "1"	0.0 0.85	0.05 10.0	V V
14	Gain adjust	Resistance to ground	260	400	Ω

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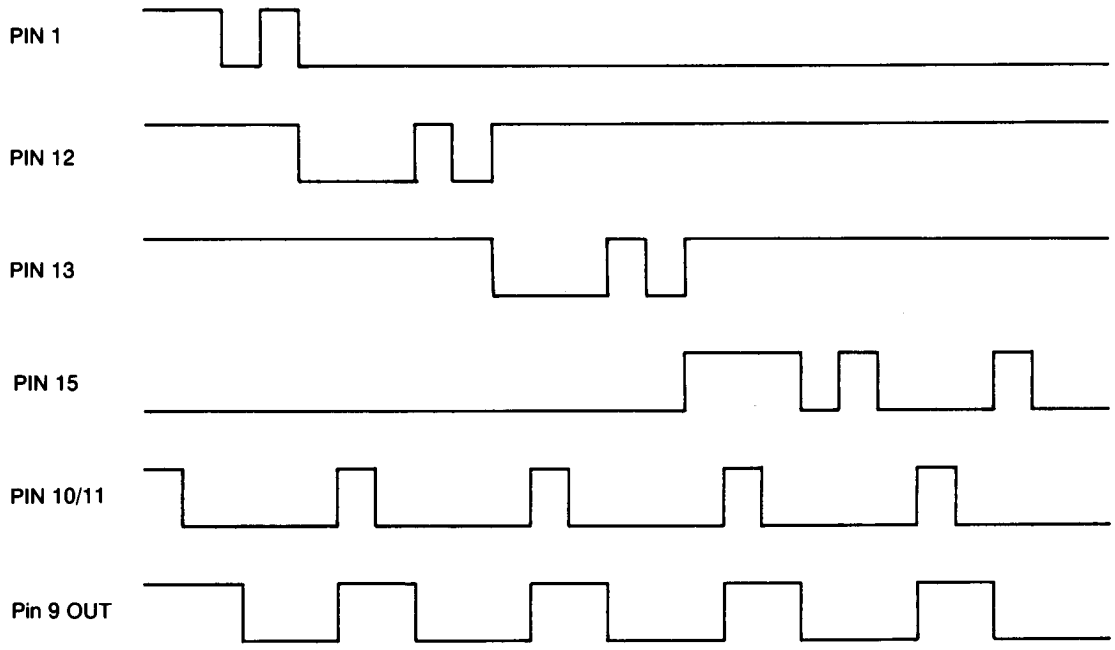
ELECTRICAL CHARACTERISTICS (cont)

Pin #	Parameter	Conditions	Limits		Units
			Min	Max	
15	Voltage sense	Logic "0" Logic "1" Input bias current: V15 = logic "1"	−1.0 0.3 0.001	−0.2 1.0 10.0	V V μA
16	Reference ground	Connect to pin 5 external to package			

TIMING DIAGRAM



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APPLICATIONS INFORMATION

Functional Description

The power available from the inverter on switching power supplies is dependent on the amount of energy fed to the inverter regulator. The 155-0067-02 allows the regulator to vary the energy delivered to the inverter by controlling the frequency at which the regulator is pulsed. This control is accomplished through the use of a variable pulse-width, monostable multivibrator, initially triggered by current-phase information fed back from the inverter to pins 10 and 11.

The multivibrator charge ramp is applied to pin 12. When this ramp moves through a level set by one of the sensing inputs, the output at pin 9 sinks drive current away from the inverter regulator until the inverter passes through a zero crossing sending a trigger pulse to either pin 10 or in 11 and the output once again is allowed to provide drive to the inverter.

The time during which the ramp at pin 12 is charging determines how long the inverter is held off. The duration of the "on" state of the multivibrator is determined by the voltage level on pin 15. If this level is low, the duration is short. As this voltage increases, the duration increases.

When a fault is detected at either pin 2 or pin 13 a capacitor externally connected to pin 1 begins to charge up. If the fault lasts longer than the time it takes for the ramp at pin 1 to reach 1 Vbe, then Q42 turns on causing a positive inverter stop trigger output at pin 8, and the inverter shuts down.

The discharge rate of the capacitor on pin 1 must be set external to the IC and must be approximately five times the charge rate.

Product Precautions

Input Protection

Reference voltage (pin 6) is developed by current driving pin 6. NEVER apply a voltage source to this pin.

Pins 1, 2, 3, 4, 10 and 11 all connect to the bases of grounded emitter transistors. When voltage driven, the current must be limited in order that damage does not occur.

The substrate voltage applied to pin 7 is typically from -2 V to -3 V in all present applications. Internal current sources have a measure of dependence on the substrate voltage. A voltage applied to pin 7 which is outside this range will inhibit the functionality of the device.

Output Loading

This device has two main outputs (pins 8 and 9). Pin 8 should never see a voltage transient greater than 15 V. Pin 9 is a current source/sink output. It must, therefore, be loaded in such a manner so as to perform both the sourcing and sinking functions interchangeably.

Power Supply Turn-on/Turn-off Sequence

Power should come up either simultaneously or with the substrate voltage (pin 7) slightly ahead of the reference current driving pin 6.

The current driving pin 6 should be removed either simultaneously or slightly ahead of the substrate voltage (pin 7).

Handling Procedures

This device is sensitive to static discharge. Care should be taken in handling.

Reliability

λ failure rate $\leq$ .02%/1K hours at 75°C Tj

AMPLIFIER

DESCRIPTION

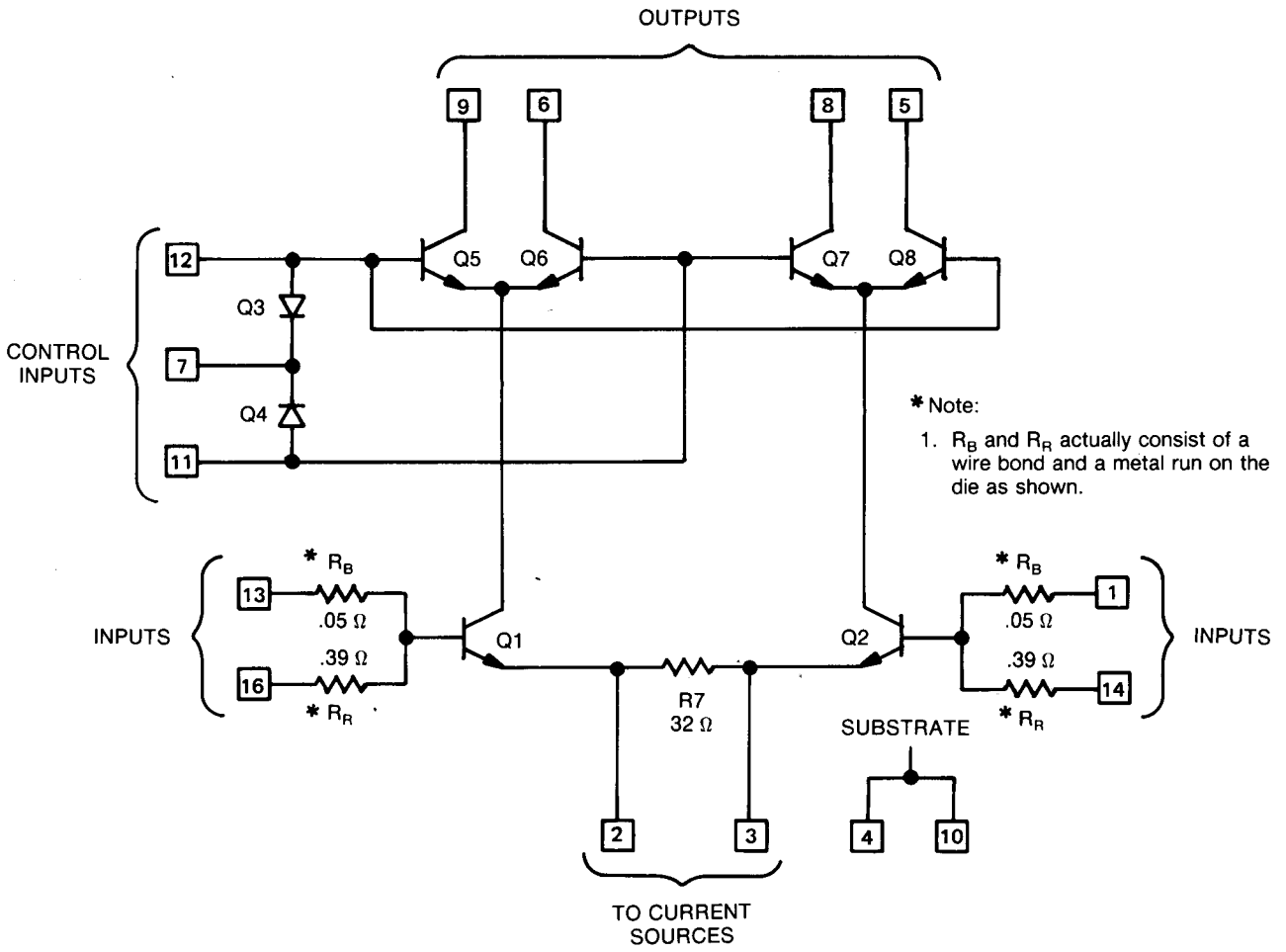
The 155-0078-10 is a monolithic integrated circuit originally designed as an Oscilloscope Vertical Amplifier.

The circuit is a differential in, differential out amplifier with variable gain capabilities. By cross-coupling the output collectors, the circuit is basically a multiplier. DC voltages applied to the control inputs can be used to vary gain from the nominal (maximum) gain through zero to the negative nominal gain. Diodes are provided on the control inputs to linearize the gain characteristics.

FEATURES

- Nominal voltage gain 2.82 (50 Ω source and loads). Set primarily by an on-chip nichrome resistor.
- Gain variable from nominal (either polarity) to zero.
- Nominal bandwidth 1.05 GHz.
- Package leads and etched circuit board can be used to obtain T-coil peaking.
- Available in three versions:
  155-0078-10 (Minipak)
  155-0273-00 (14-pin DIP w/o nichrome resistors)
  155-0274-00 (14-pin DIP) (slower)

SCHEMATIC

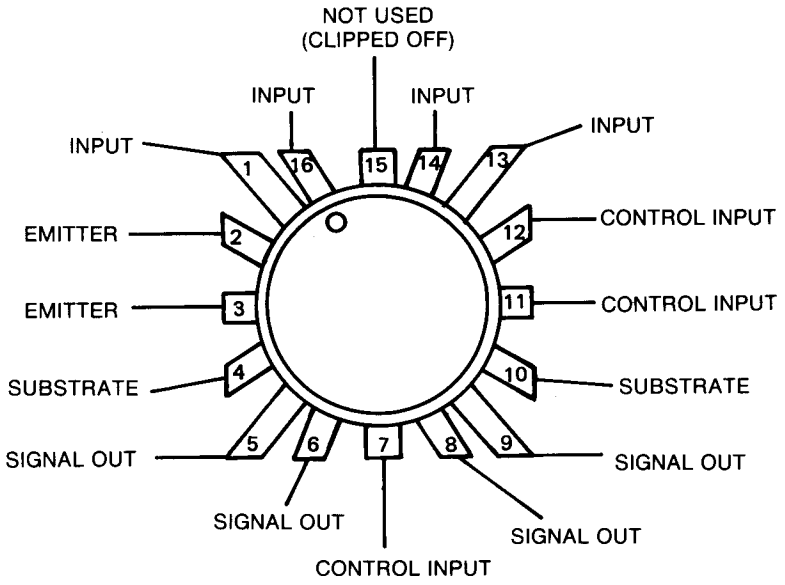


ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	NOTES	VALUES	UNITS
$V_{out\text{-}sub\ MAX}$	Maximum voltage of the outputs (pins 5, 6, 8, 9) relative to the substrate (pin 4).	Prevents collector-substrate breakdown of Q5, Q6, Q7, Q8.	19	V
$V_{out\text{-}cont\ MAX}$	Maximum voltage of the outputs (pins 5, 6, 8, 9) relative to the control inputs (pins 11, 12).	Prevents collector-base breakdown of Q5, Q6, Q7, Q8.	7	V
$V_{cont\text{-}input\ MAX}$	Maximum voltage at the control inputs (pins 11, 12) relative to inputs (pins 1, 13, 14, 16).	Prevents collector-base breakdown of Q1 and Q2.	8	V
$V_{sub\text{-}input\ MAX}$	Maximum voltage of the substrate (pin 4) relative to the inputs (pins 1, 13, 14, 16).	Substrate voltage must be held more negative than any collector in circuit.	0	V
$V_{RQ3\ MAX}$	Maximum voltage from pin 7 to pin 11 or 12.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
$V_{R11\text{-}R12\ MAX}$	Maximum voltage from pin 11 to 12 or from pin 12 to pin 11.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
$V_{EB\ MAX}$	Maximum voltage from pin 2 to pin 13 or 16; or from pin 3 to pins 1 or 14.	Maximum base-emitter reverse voltage to avoid degradation.	2	V
I_{MAX}	Maximum current, pins 2 or 3.	40 mA total.	20*	mA
P_{MAX}	Maximum power dissipation.	75°C ambient.	270	mV
$T_{OPERATING}$	Operating temperature range.		0 to 80	°C
$T_{STORAGE}$	Storage temperature range.		−55 to +125	°C
$T_{j\ MAX}$	Maximum junction temperature.		125	°C

*** Contact Applications Engineering, IC Manufacturing, if 20 mA is to be exceeded.**

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN	MAX	UNITS
BV_{CEO} Q1, Q2, at 200 μA	4.4		V
BV_{CEO} Q5, Q6, Q7, Q8 at 200 μA	4.4		V
$BV_{CEO\ SUS}$ Q1, Q2 at 10 mA	4.9		V
$BV_{CEO\ SUS}$ Q5, Q6, Q7, Q8 at 10 mA	4.9		V
SUBSTRATE VOLTAGE in operating configuration		−15	V
INPUT BIAS CURRENT Q1 or Q2 (16 mA emitter current)	64	225	μA
NORMAL OFFSET (OUTPUT)	−14	+14	mV
INVERT OFFSET (OUTPUT)	−14	+14	mV
NORMAL GAIN	2.68	2.96	
INVERT GAIN	2.68	2.96	
NORMAL-INVERT GAIN MATCH	−0.5	+0.5	%
NULL OFFSET (Output offset in null condition)	−10	+10	mV
NULL GAIN	−.14	+.14	
50% GAIN TOLERANCE	.49	.51	$X(AV_{NORM})$
OFF FEEDTHRU (Q5 & Q8 leakage)	−200	+200	μV
MEASURED RISETIME Measurement system risetime less than 100 ps		355	ps

PARAMETRIC DEFINITIONS

The 0078 is specified in three different operating conditions: NORMAL, INVERT and NULL.

In the NORMAL condition, Q5 and Q8 are conducting and Q6 and Q7 are not.

In the INVERT condition, Q6 and Q7 are conducting and Q5 and Q8 are not.

In the NULL condition, Q5, Q6, Q7 and Q8 are all conducting equally.

APPLICATIONS INFORMATION

Output Stage Considerations

Pin 11 and 12 can be voltage driven and pin 7 left open (Figure 1) if gain linearity as a function of control voltage is not critical. The voltage applied on pins 11 or 12 should be 1.2 to 3.7 volts above the quiescent voltage on pins 1, 13, 14, or 16 for conducting output transistors. For nonconducting output transistors pin 11 or 12 can be at a lower potential than this. Absolute maximum ratings must be observed, however. For the case of pin 11 and 12 voltage driven and pin 7 open, gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{\exp\left(\frac{qV_{12}}{kT}\right) - \exp\left(\frac{qV_{11}}{kT}\right)}{\exp\left(\frac{qV_{12}}{kT}\right) + \exp\left(\frac{qV_{11}}{kT}\right)}\right]$$

where $A_{V\,NORM}$ = Normal Gain
V_{11} = voltage applied on pin 11
V_{12} = voltage applied on pin 12
$\frac{kT}{q}$ = 26 mV at room temperature

If gain linearity as a function of control voltage is critical, pin 11 and 12 should be current driven and pin 7 returned to a voltage so as to set pin 11 and 12 voltage to the proper level as mentioned above. Figure 2 shows this type hookup. Current driving these inputs linearizes the gain by making use of the exponential current-voltage relationship of the diodes Q3 and Q4 to cancel that of the output transistors. The gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{I_{12} - I_{11}}{I_{12} + I_{11}}\right]$$

where I_{11} = current into pin 11
I_{12} = current into pin 12

If variable gain of only a single polarity is desired, one pair of outputs can be used and the other pair connected to separate unused leads as in Figure 3.

If fixed maximum gain is desired, one pair of outputs can be left open as in Figure 4.

In applications where the output is to be switched from one output pair to another, the difference in offset voltage between the two outputs should not be specified any tighter than 28 mV (the sum of normal and invert offset specs).

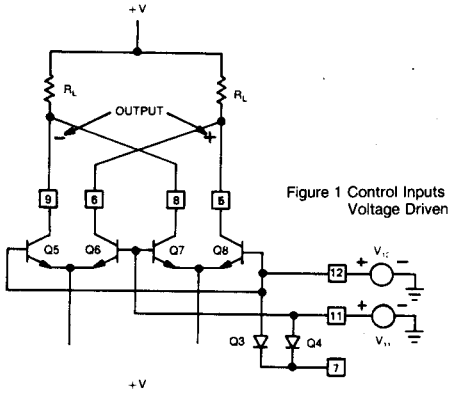


Figure 1 Control Inputs Voltage Driven

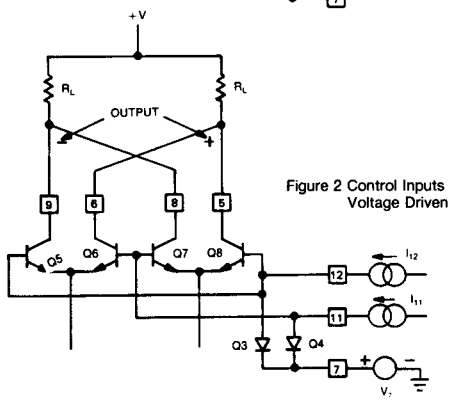
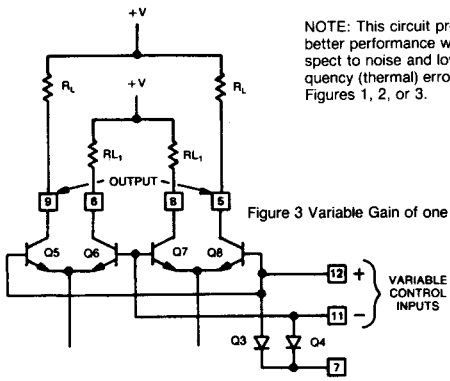
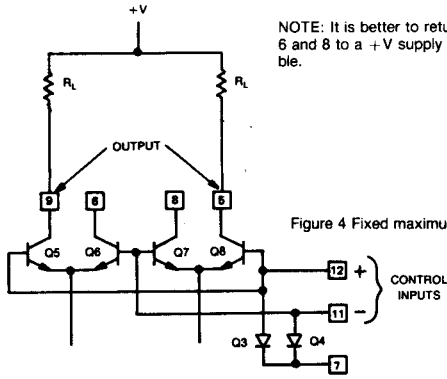


Figure 2 Control Inputs Voltage Driven



NOTE: This circuit provides better performance with respect to noise and low frequency (thermal) errors than Figures 1, 2, or 3.

Figure 3 Variable Gain of one polarity only



NOTE: It is better to return 6 and 8 to a +V supply if possible.

Figure 4 Fixed maximum gain

Input Stage Considerations

The bias current (pin 2 and 3 current) should not exceed 20 mA per side or a decrease in the life of the part may result.

For full bandwidth, T-coil peaking must be used. Package and etched circuit board inductances can be used in the realization of this bridged T circuit[1].

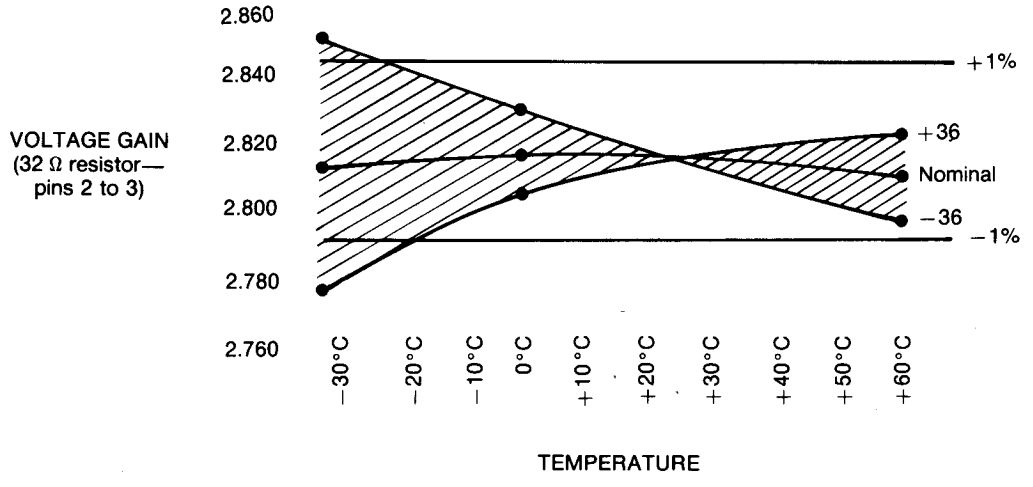
Standing current through pin 16 to 13 and pin 1 to 14 will cause a DC drop due to the run and bond wire resistance in their leads. This resistance provides some intentional improvement in gain vs. temperature and may need to be considered in biasing calculations.

Thermal effects due to signal dependent power dissipation changes in Q_1 and Q_2 cause the low frequency gain to exceed mid band gain by $\approx$1% with Q_1, Q_2 at 15 mA, 2.4 V.

[1]See John Addis' article in *Electronics Magazine* June 5, 1972.

Typical Performance Graph
(not a specification, for information only)

155-0078 GAIN Vs TEMPERATURE



PRODUCT PRECAUTIONS

Input Protection

Input base-emitter voltages should not exceed 2 volts in the negative direction and 1 volt in the positive direction.

Output Loading

Outputs should be limited to less than those listed in Absolute Maximum Ratings.

Power Supply Turn-On/Turn-Off Sequence

Substrate voltage should be turned on coincident with or before the other voltages.

Handling Procedures

Static sensitive handling procedures should be implemented for this part.

RELIABILITY

λ. failure rate $\leq$ .02%/1K hours at 75°C Tj.

$\Theta jc = 87°C/W$.

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TRIGGER CIRCUIT

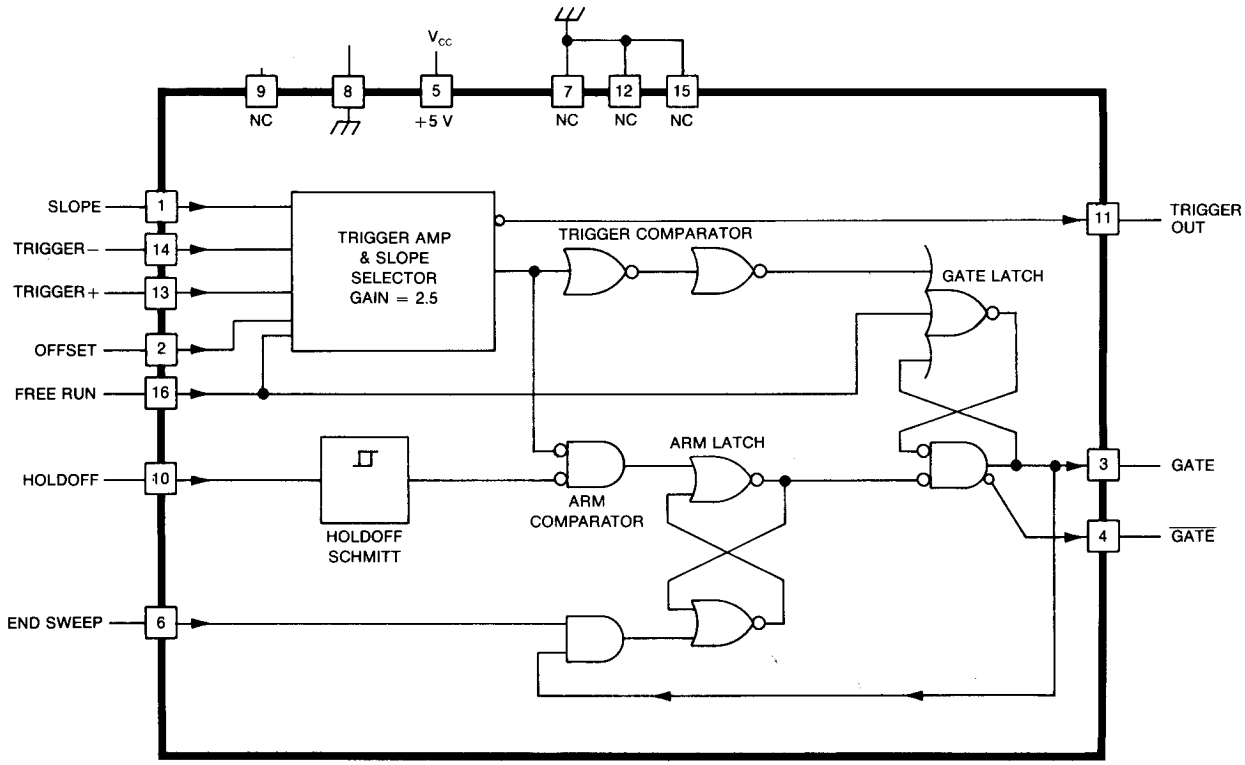
DESCRIPTION

The 155-0109-01 is a 350 MHz trigger circuit. It can be used by itself or in conjunction with the 155-0126-00 trigger amplifier, channel switch and peak to peak auto I.C.

FEATURES

- 350 MHz operation
- ECL input and output levels (slope input is T^2L)
- Trigger slope select
- Compatible with the 155-0126-00 trigger amplifier, channel switch

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

V_{CC} (Pin 5) ..... +5.25 Volts
Input Voltage (All Inputs) ..... 0 Volts to V_{CC}
Storage Temperature (T_{SG}) ..... −55°C to 125°C
Operating Ambient Temperature (T_A) ..... −15°C to +75°C
Maximum Power Dissipation (P_D) ..... 600 mW

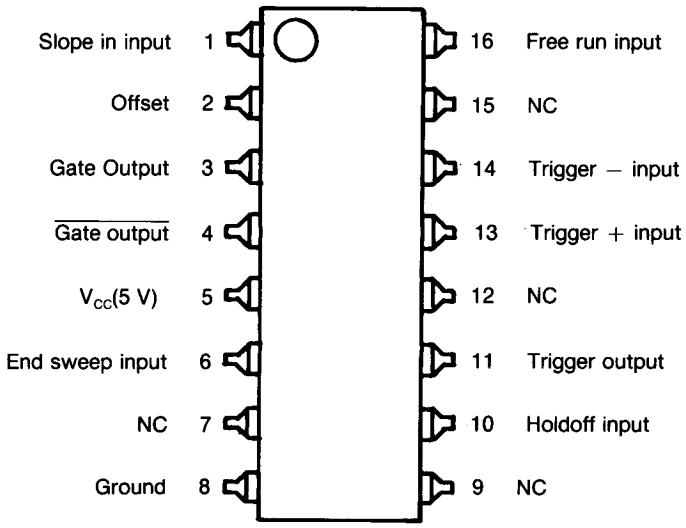
Derating Factor (Above 70°C Ambient) ..... 11 mW/°C

NOTE 1: **Maximum Die Temperature NOT To Exceed 125°C.**

NOTE 2: **The Trigger Out (Pin 11) is NOT specified herein. It thas the following characteristics:**

- **The Gain from the Trigger Inputs to Pin 11 is 2.5**
- **Pin 11 output range is ECL and**
- **Phase, relative to the Trigger Inputs depends on Slope setting.**

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PARAMETER	PIN	MIN	MAX	UNITS
Power Supply Current (note 4)	8	70	120	mA
+ Slope, + Trigger Input Bias Current (note 5)	13	−100	100	μA
+ Slope, − Trigger Input Bias Current (note 5)	14	−100	100	μA
+ Slope, Trigger Input Offset Current (+ Trigger Input Bias Current Less—Trigger Input Bias Current) (computed)	13, 14	−25	25	μA
− Slope, + Trigger Input Bias Current (note 6)	13	−100	100	μA
− Slope, − Trigger Input Bias Current (note 6)	14	−100	100	μA
− Slope, Trigger Input Offset Current (+ Trigger Input Bias Current Less—Trigger Input Bias Current (computed)	13	−25	25	μA
Hold-Off Input Current (note 4)	10	−200	200	μA
End Sweep Input Current (Note 1) (note 4)	6	−200	200	μA
Free Run Input Current (note 7)	16	0	500	μA
Slope In Input Current (note 8)	1	−2.0	0	mA
Slope In Input Current (note 9)	1	−40	40	μA

ELECTRICAL CHARACTERISTICS (cont)

PARAMETER	PIN	CONDITIONS	MIN	MAX	UNITS
Gate Out (V_{OH}) High Voltage	3	I_{OH} = −3 mA, Perform Steps 1 through 3 of the Truth Table, then measure (Ignore Note 2)	4.0	4.3	V
Gate Out Low Voltage (V_{OL})	3	I_{OL} = 1 mA, Perform Steps 17 through 19 of the Truth Table, then measure (Ignore Note 2)	3.2	3.5	V
$\overline{\text{Gate}}$ Out High Voltage (V_{OH})	4	I_{OH} = −3 mA, Perform Steps 17 through 19 of the Truth Table, then measure (Ignore Note 2)	4.0	4.3	V
$\overline{\text{Gate}}$ Out Low Voltage (V_{OL})	4	I_{OL} = −1 mA, Perform Steps 1 through 3 of the Truth Table, then measure (Ignore Note 2)	3.2	3.5	V
+ Trigger Absolute Offset	13, 14	Perform Steps 1 through 4 of Table 1 repeatedly, adjusting the input 1 and 0 levels independently until the arm and trigger thresholds are determined. The + Trigger Absolute Offset = ($V_{Trigger}$ − V_{Arm})/2 −3.8 Volts.	−40	+40	mV
+ Slope Hysteresis	13, 14	Use data obtained in + trigger absolute offset Hysteresis = $V_{Trigger}$ − V_{Arm}	25	50	mV
− Trigger Absolute Offset	13, 14	Perform Steps 1 through 4 of Table 2 repeatedly, adjusting the input 1 and 0 levels independently until the arm and trigger thresholds are determined. The − Trigger Absolute Offset = (V_{Arm} + $V_{Trigger}$)/2 − 3.8 Volts.	−40	+40	mV
− Slope Hysteresis	13, 14	Use data obtained in − trigger absolute offset Hysteresis = V_{Arm} − $V_{Trigger}$	25	50	m
+ Trigger Slope In, − Trigger Slope Offset	13, 14	(Offset = (+Trigger Slope Absolute Offset less −Trigger Slope Absolute Offset)	−40	+40	mV*
Propagation Delay (T_{PD+})	3, 13, 14	See Figure 1		4.0	nS

***Adjustable to ±4 mV with offset adjust (Pin 2), with an offset range of 0.5 to 4.5 Volts.**

TRUTH TABLE
(See Note 3)
INPUTS

Step	Function	Slope Pin 1 (T^2L)	End Sweep Pin 6 (ECL)	Holdoff Pin 10 (ECL)	+IN Pin 13	−IN Pin 14	Free Run Pin 16	Gate Pin 3	Gate Pin 4	Notes
1	RESET	0c	1a	1a	0a	1a	0b	VOL	VOL	Power Supply Pin 5 + 5 V Pin 8 Gnd.
2	ARM	0c	0a	0a	0a	1a	0b	VOL	VOH	
3	+ Trigger	0c	0a	0a	1a	0a	0b	VOH	VOL	
4	LATCH	0c	0a	0a	0a	1a	0b	VOH	VOL	INPUT VOLTAGE LEVEL CODING
5	$\overline{\text{RESET}}$	0c	1a	0a	0a	1a	0b	VOH	VOL	0a 3.55 V 0b 3.4 V
6	RESET	0c	1a	1a	0a	1a	0b	VOL	VOH	0c 0.8 V 1a 3.95 V
7	ARM	0c	0a	0a	0a	1a	0b	VOL	VOH	
8	$\overline{\text{DISARM}}$	0c	0a	1a	0a	1a	0b	VOL	VOH	
9	$\overline{\text{DISARM}}$	0c	1a	1a	0a	1a	0b	VOL	VOH	
10	LATCH	0c	0a	1a	0a	1a	0b	VOL	VOH	
11	+ Trigger	0c	0a	1a	1a	0a	0b	VOH	VOL	OUTPUT VOLTAGE LEVEL CODING VOL 3.2 V to 3.5 V
12	LATCH	0c	0a	1a	0a	1a	0b	VOH	VOL	VOH 4.0 V to 4.3 V
13	RESET	1b	1a	1a	0a	1a	0b	VOL	VOH	(See Note #2)
14	ARM	1b	0a	0a	1a	0a	0b	VOL	VOH	
15	− Trigger	1b	0a	0a	0a	1a	0b	VOH	VOL	
16	LATCH	1b	0a	0a	1a	0a	0b	VOH	VOL	
17	RESET	1b	1a	1a	1a	0a	0b	VOL	VOH	
18	$\overline{\text{ARM}}$	1b	0a	1a	0a	1a	0b	VOL	VOH	
19	$\overline{\text{TRIGGER}}$	1b	0a	0a	0a	1a	0b	VOL	VOH	
20	FREE RUN	1b	0a	0a	0a	1a	1a	VOH	VOL	

TABLE #1

Step	Function	INPUTS						OUTPUTS
		Slope (Pin 1)	End Sweep (Pin 6)	Holdoff (Pin 10)	+ Trigger In (Pin 13)	−Trigger In (Pin 14)	Free Run (Pin 16)	Gate (Pin 3)
1	RESET	.8 V	3.95 V	3.95 V	LOGIC 0	3.8 V	3.4 V	3.2 V to 3.5 V
2	ARM	.8 V	3.55 V	3.55 V	LOGIC 0	3.8 V	3.4 V	3.2 V to 3.5 V
3	+ TRIGGER	.8 V	3.55 V	3.55 V	LOGIC 1	3.8 V	3.4 V	4.0 V to 4.3 V
4	LATCH	.8 V	3.55 V	3.55 V	LOGIC 0	3.8 V	3.4 V	4.0 V to 4.3 V

TABLE #2

Step	Function	INPUTS						OUTPUTS	
		Slope (Pin 1)	End Sweep (Pin 6)	Holdoff (Pin 10)	+ Trigger In (Pin 13)	−Trigger In (Pin 14)	Free Run (Pin 16)	Gate (Pin 3)	Gate (Pin 4)
1	RESET	2.0 V	3.95 V	3.95 V	LOGIC 0	3.8 V	3.4 V	3.2 V to 3.5 V	
2	ARM	2.0 V	3.55 V	3.55 V	LOGIC 1	3.8 V	3.4 V	3.2 V to 3.5 V	
3	− TRIGGER	2.0 V	3.55 V	3.55 V	LOGIC 0	3.8 V	3.4 V	4.0 V to 4.3 V	
4	LATCH	2.0 V	3.55 V	3.55 V	LOGIC 1	3.8 V	3.4 V	4.0 V to 4.3 V	

NOTE 1: Gate Out (Pin 3) held at 5 Volts after Power Supply settles at +5 Volts.

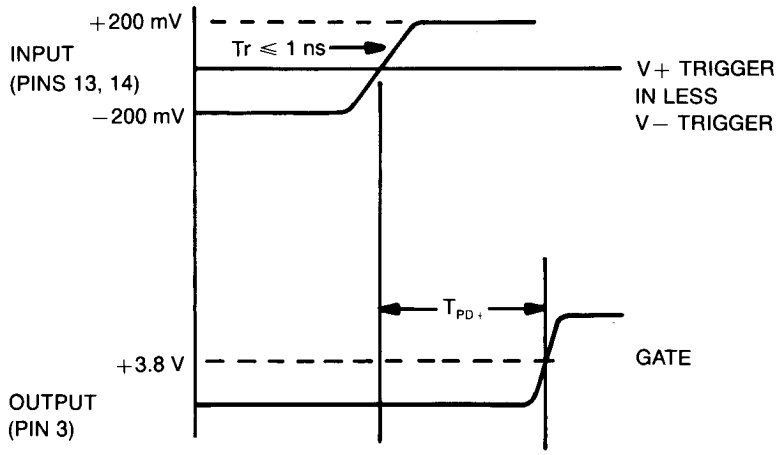
NOTE 2: Pins 3 and 4 loaded with a 2kΩ resistor connected from Output Pin to Ground during testing.

NOTE 3: The Truth Table for Parameter 13 to be accomplished without Power Supply interruption.

CONDITIONS

	+ Trigger In (Pin 13)	− Trigger In (Pin 14)	Free Run In (Pin 16)	End Sweep In (Pin 6)	Slope In (Pin 1)	Holdoff In (Pin 10)
Note 4	3.55 V	3.95 V	3.4 V	3.95 V	.8 V	3.95 V
Note 5	3.8 V	3.8 V	3.4 V	3.95 V	.8 V	3.95 V
Note 6	3.8 V	3.8 V	3.4 V	3.95 V	2.0 V	3.95 V
Note 7	3.55 V	3.95 V	3.95 V	3.95 V	.8 V	3.95 V
Note 8	3.55 V	3.95 V	3.4 V	3.95 V	0 V	3.95 V
Note 9	3.55 V	3.95 V	3.4 V	3.95 V	2.4 V	3.95 V

FIGURE 1



Reliability

λ, failure rate ≤.02%/1K hours at 75°T_j

Thermal impedance, θ_{DA} = 65°C/W

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QUAD OPERATIONAL AMPLIFIER

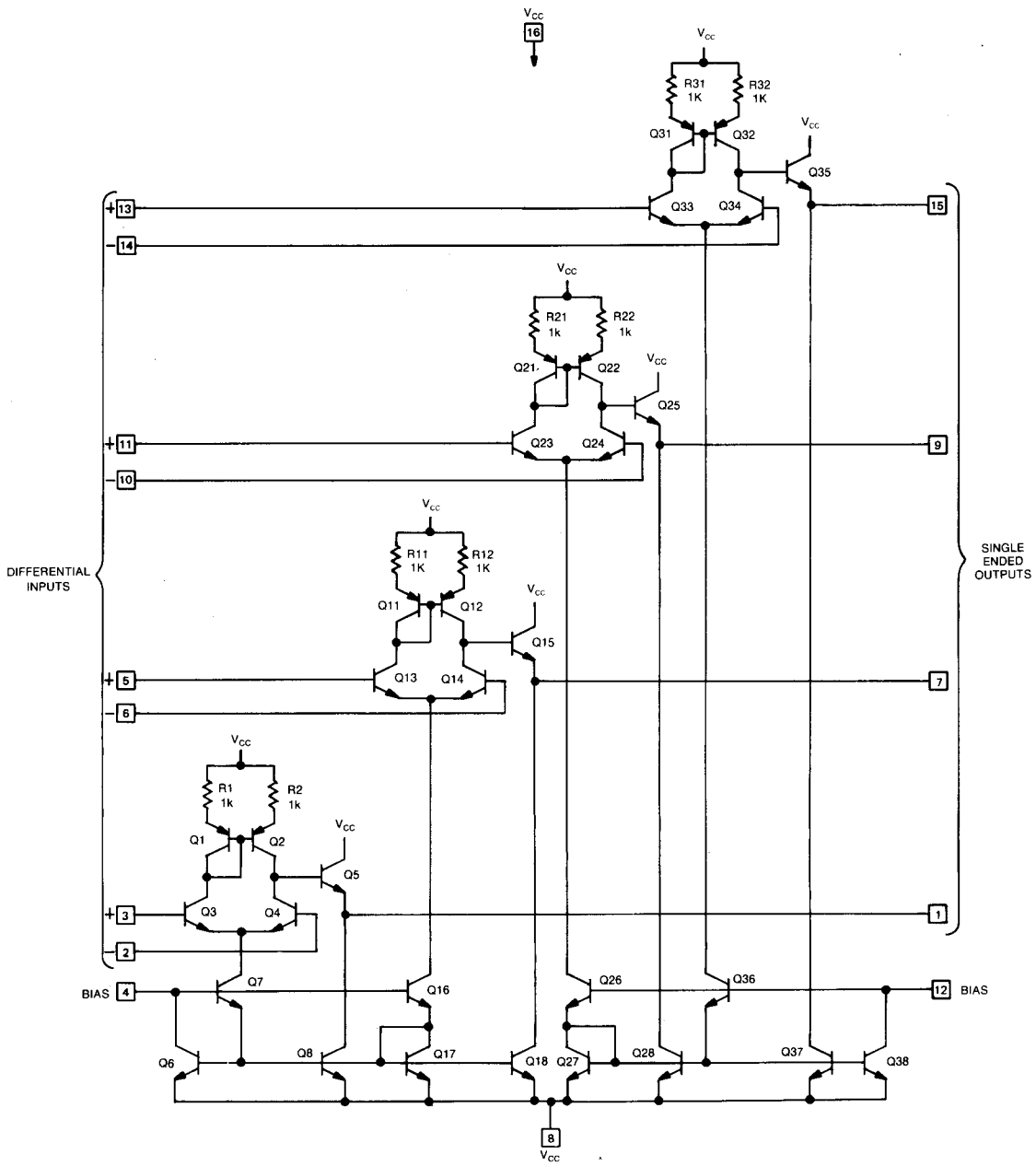
DESCRIPTION

The 155-0116-00 is a silicon monolithic quad operational amplifier. It comes in a ceramic 16 pin DIP.

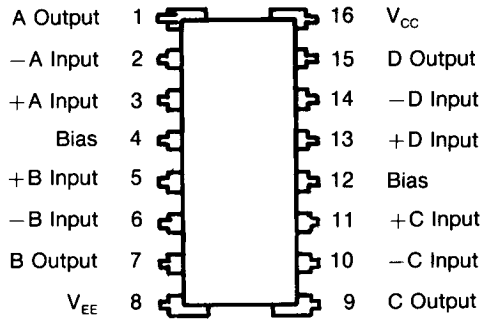
FEATURES

- ±5 V to ±15 V power supply range
- 80 MHz gain bandwidth product
- 20 mA output bandwidth product
- No compensation required
- Open loop gain 3300 typical
- 5 mV input offset voltage
- Available in two versions:
  155-0035-00 (plastic DIP)
  155-0116-00 (ceramic DIP)

SCHEMATIC


VCC
16
R31
1K
R32
1K
Q31
Q32
Q35
Q33
Q34
13
14
15
R21
1k
R22
1k
Q21
Q22
Q25
Q23
Q24
11
10
9
R11
1K
R12
1K
Q11
Q12
Q15
Q13
Q14
5
6
7
R1
1k
R2
1k
Q1
Q2
Q5
Q3
Q4
3
2
1
DIFFERENTIAL
INPUTS
SINGLE
ENDED
OUTPUTS
BIAS
4
Q7
Q16
Q26
Q36
12
BIAS
Q6
Q8
Q17
Q18
Q27
Q28
Q37
Q38
8

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS*	MIN	MAX	UNITS
V_{CC}	14.25	15.75	V
V_{EE}	−14.25	−15.75	V
Open Loop Voltage Amplification Condition: See Figure 1	1000		
Input Offset Voltage Condition: R_L more than 100KΩ. Input connected to output; (+) Input grounded. Measure output voltage.		±5	mV
Risetime Condition: See Figure 2.		60	nS
Closed Loop Voltage Amplification Condition: See Figure 3.	9.70		
Output Voltage Swing Condition: Output Voltage Swing will not go more than 1.0 V negative of (−) Input.	±12.0		V
Noise Condition: Referred to Input.		100	μV/ peak to peak

***The circuit conditions at which these parameter values were tested are:**
V_{CC} = +15 V, V_{EE} = −15 V; I_{REF} = 0.25 mA. All these values ±5.0%. T_A = 0 to +70°C.

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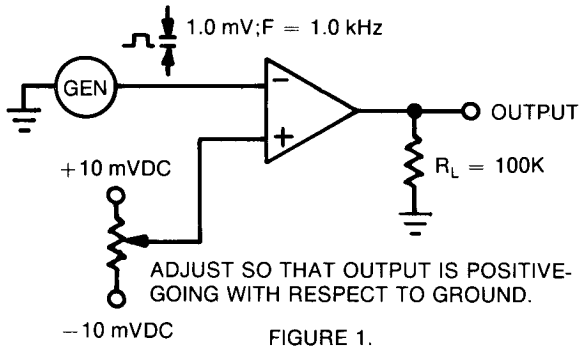

FIGURE 1.

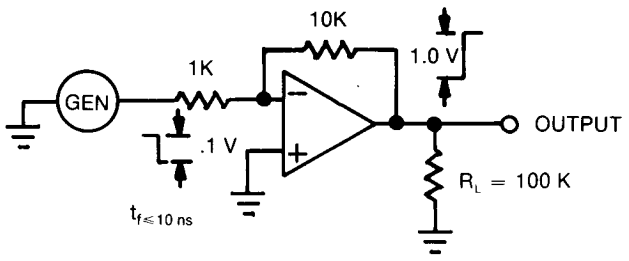

FIGURE 2.

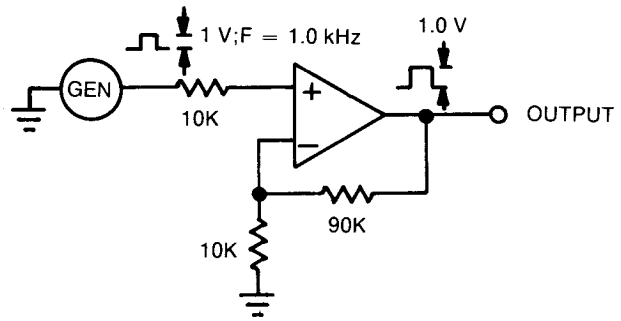

FIGURE 3

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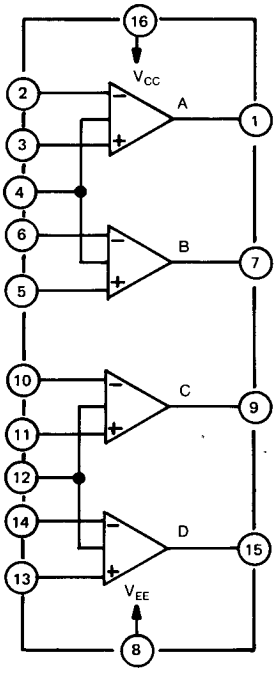
BLOCK DIAGRAM



ABSOLUTE MAXIMUMS*

SYMBOLS	IDENTIFICATION	VALUES	UNITS
	Difference between V_{CC} and V_{EE}	32	V
$V_{DN.DIFF}$	Differential Input Voltage	7	V
I_{REF}	Reference Current	500	μA
I_{OUT}	Output Current	20	mA
$T_{STORAGE}$		−55 to 125	°C
$T_{OPERATING}$		0 to 70	°C
P_D	Maximum Power Dissipation	375	mW
	Maximum Junction Temperature	125	°C

***Since this device does not have internal current limiting, the circuits being driven by pins 1, 7, 9 and 15 should have some form of current limiting to keep from exceeding the Absolute Maximum Rating (I_{OUT}) of 20 mA for this device.**

APPLICATIONS INFORMATION

Reliability

λ, Failure Rate, .02%/1K hours at 75°C T_j

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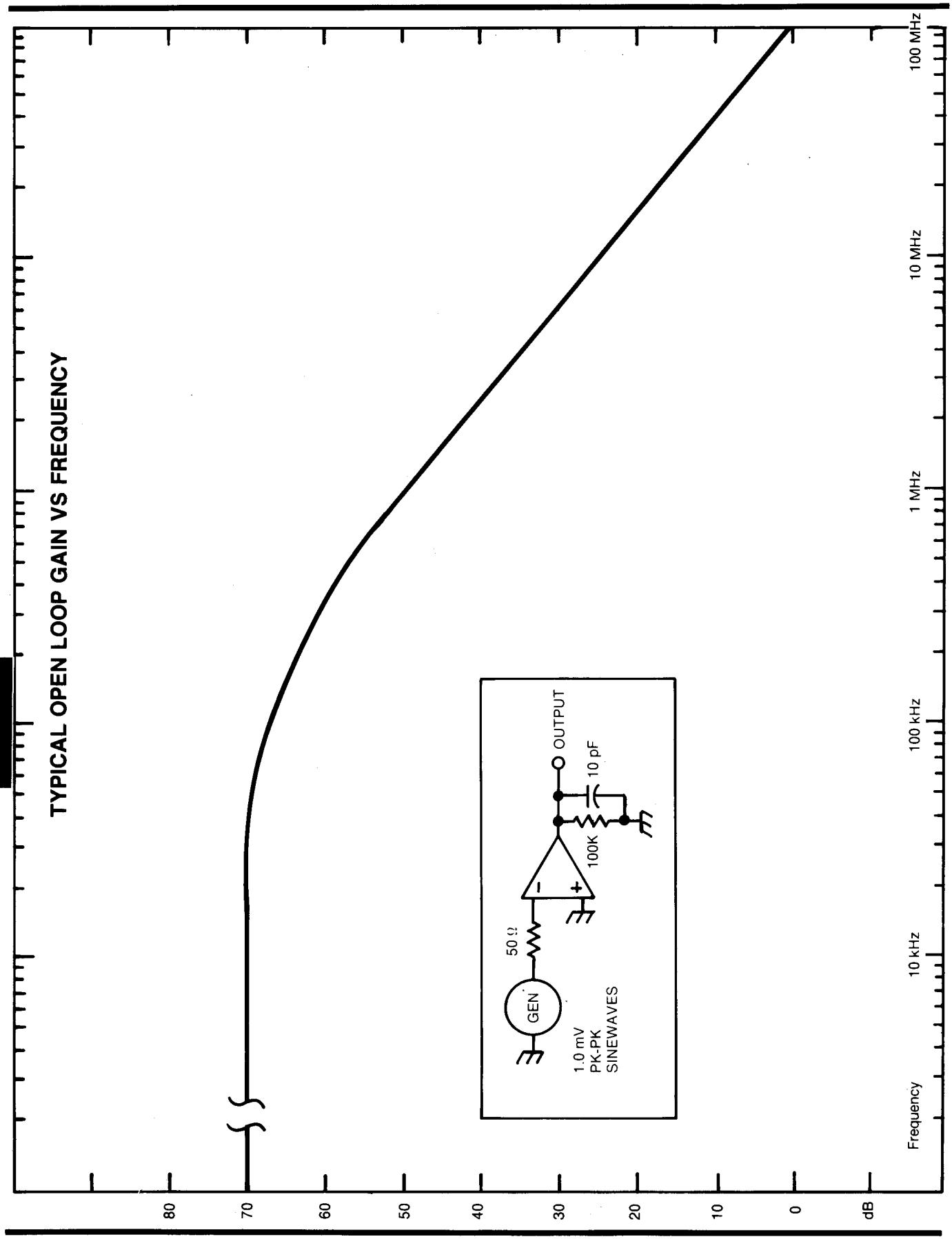

TYPICAL OPEN LOOP GAIN VS FREQUENCY
80
70
60
50
40
30
20
10
0
dB
Frequency
10 kHz
100 kHz
1 MHz
10 MHz
100 MHz
OUTPUT
10 pF
100K
50 Ω
GEN
1.0 mV
PK-PK
SINEWAVES

SWEEP CONTROL

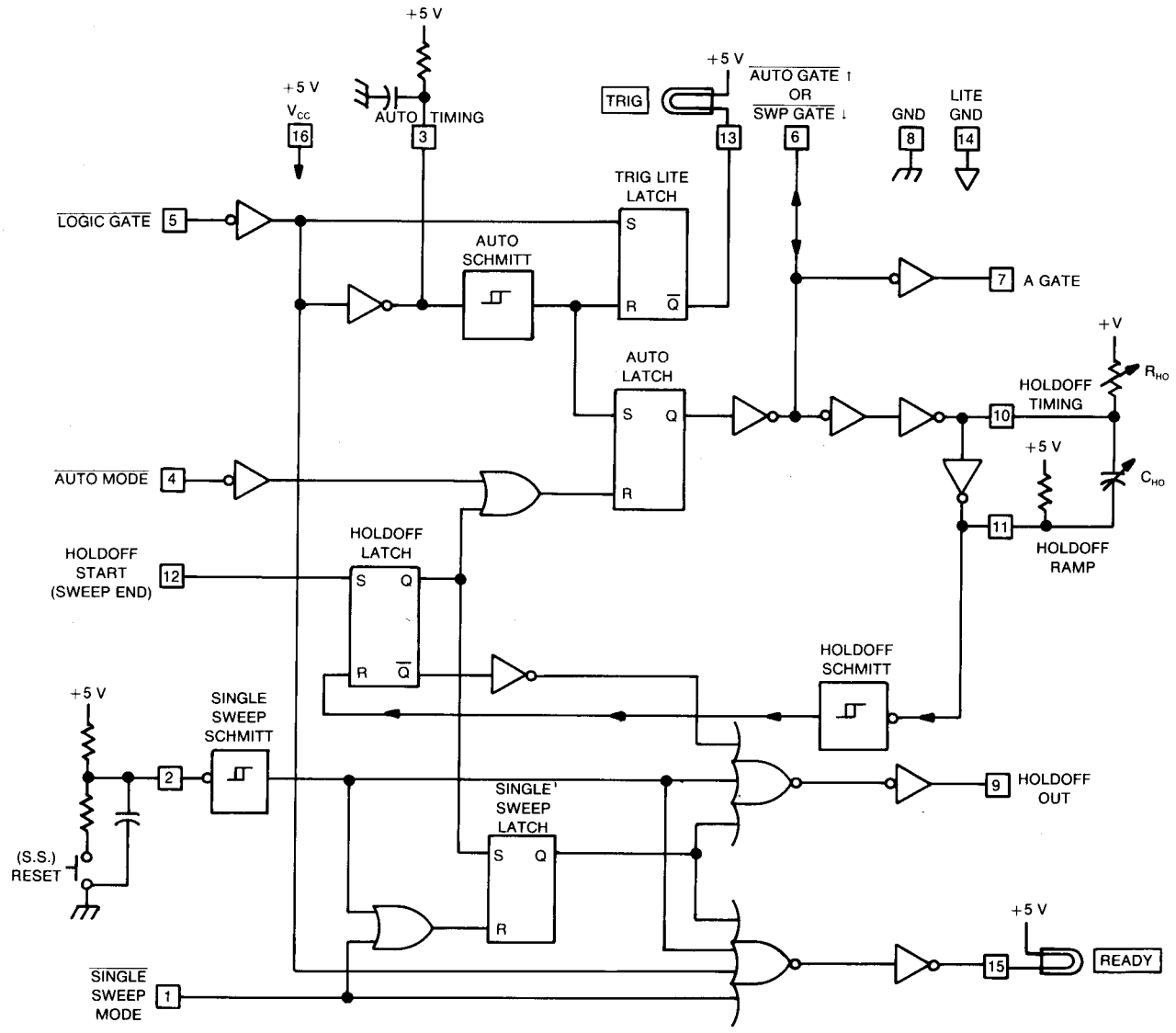
DESCRIPTION

The 155-0122-00 is a Monolithic Integrated Sweep Control Circuit designed to interface with the 155-0123-00 Sweep and Delay Pickoff IC and the 155-0196-00 Trigger IC to form a complete Horizontal System.

FEATURES

- Miller hold-off timing circuit
- Single sweep lockout circuit
- Triggered and single sweep ready light lamp drivers
- Single sweep reset debounce circuit
- Auto timing circuit
- "A" gate output

BLOCK DIAGRAM



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUE	UNITS
	Input voltage. Pins 1, 4, 5, 6, 10, and 12)	−0.3 to V_{CC}	V
	Input voltage. (pins 2, 3, and 11)	−0.3 to V_{CC} +0.5	V
	Output sink current. (Pins 6, 7, 9, and 11)	6.0	mA
	Lamp sink current. (Pins 13 and 15)	100	mA
	Lamp V_{CC} (Pins 13 and 15)	+7.5	V
	Sink current. (Pin 10)	20	mA
	Input current. (Pins 1, 2, 3, 4, 5, 10, and 12)	5	mA
	V_{CC} (Pin 16)	+7.5	V
	Light ground. (Pin 14)	−0.2 to +0.2	V
T_{sg}	Storage temperature	−55 to +125	°C
T_A	Operating ambient temperature	−15 to +85	°C
P_D	Maximum power dissipation	250	mW

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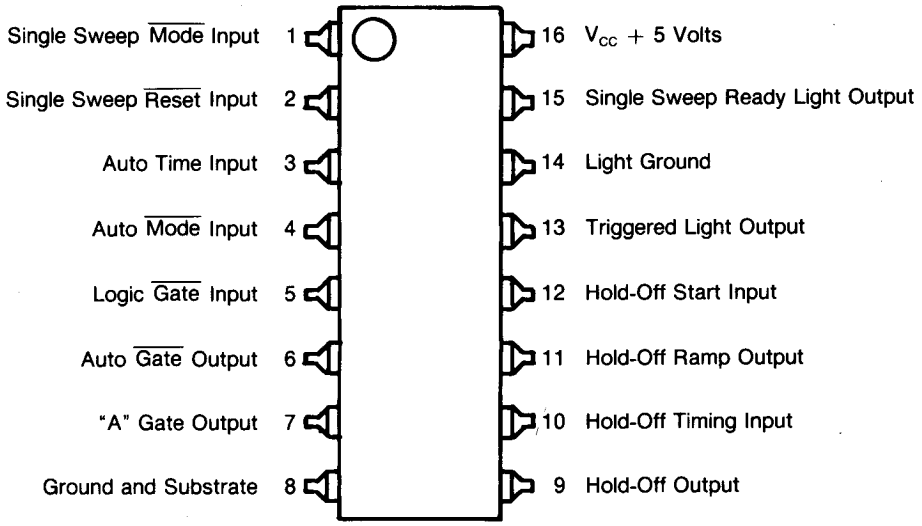
PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN	MAX	UNITS
V_{CC} current		35	mA
Input logical "0" current (Pins 1, 4, and 5)	−1.7	−5.0	mA
Input logical "0" voltage (Pins 1, 4, and 5)	0.0	0.5	V
Input logical "1" current (Pins 1, 4, and 5)	−100	0	μA
Single sweep reset positive threshold (Pin 2)	2.6	3.8	V
Timing pin input currents (See note 1) (Pins 2, 3)	0	1.5	μA
Auto timing threshold voltage (Pin 3)	2.8	4.0	V
Output logical "0" voltage (Pin 6, in which pin 6 input current = 4.0 mA)	0.0	0.5	V
Output logical "1" leakage current (Pin 6, in which pin 6 voltage = 5.6 V)	−300	+300	μA
Output logical "0" voltage (Pins 7, 9, in which pins 7, 9 input current = 2.0 mA)	0.0	0.5	V
Output logical "1" current (Pin 7, in which pins 7, 9 voltage = 1.0 V)	−5.0	−1.0	mA
Hold-off timing leakage curent (See note 2) (Pin 10)	−2	+2	μA
Hold-off ramp leakage curent (Pin 11, in which pin 11 voltage = 5.0 V)	−100	+100	μA
Hold-off ramp trip point (Pin 11)	1.7	2.3	V
Hold-off start logical "0" voltage (Pin 12)	0.0	0.5	V
Light driver (V_{SAT}) (Pins 13, 15 in which pins 13, 15 current = 60 mA)	0.0	0.6	V
Auto timing source resistance (Pin 3)	20		KΩ
Hold-off start propagation delay (See note 3) (Pins 9, 12)	100 (typ)		nSec
"A" gate propagation delay (See note 4) (Pins 6, 7)	50 (typ)		nSec
Single sweep $\overline{\text{reset}}$ negative threshold (Pin 2)	1.5	2.5	V

NOTE 1: With a 500 kΩ source resistance, the Single Sweep Reset Positive Threshold maximum increases to 4.25 V and the Auto Timing Threshold maximum increases to 4.25 V.

NOTE 2: With 1.7 MΩ OHMS from PIN 10 to +5.0 V, Pin 11 current must be equal to or more than +4.0 mA.

NOTE 3: Delay measured between Pin 12 and Pin 9. See Test Diagram, Figure 1.

NOTE 4: Delay measured between (−) edge of Pin 6 and resulting (+) edge of Pin 7. See Test Diagram, Figure 2.

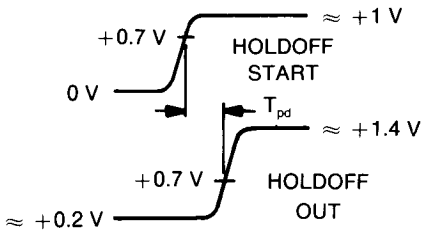


FIGURE 1

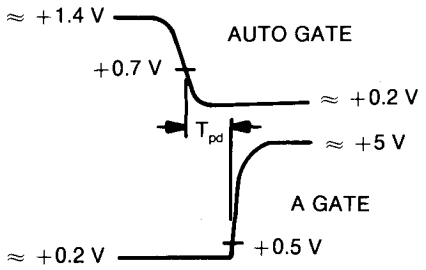
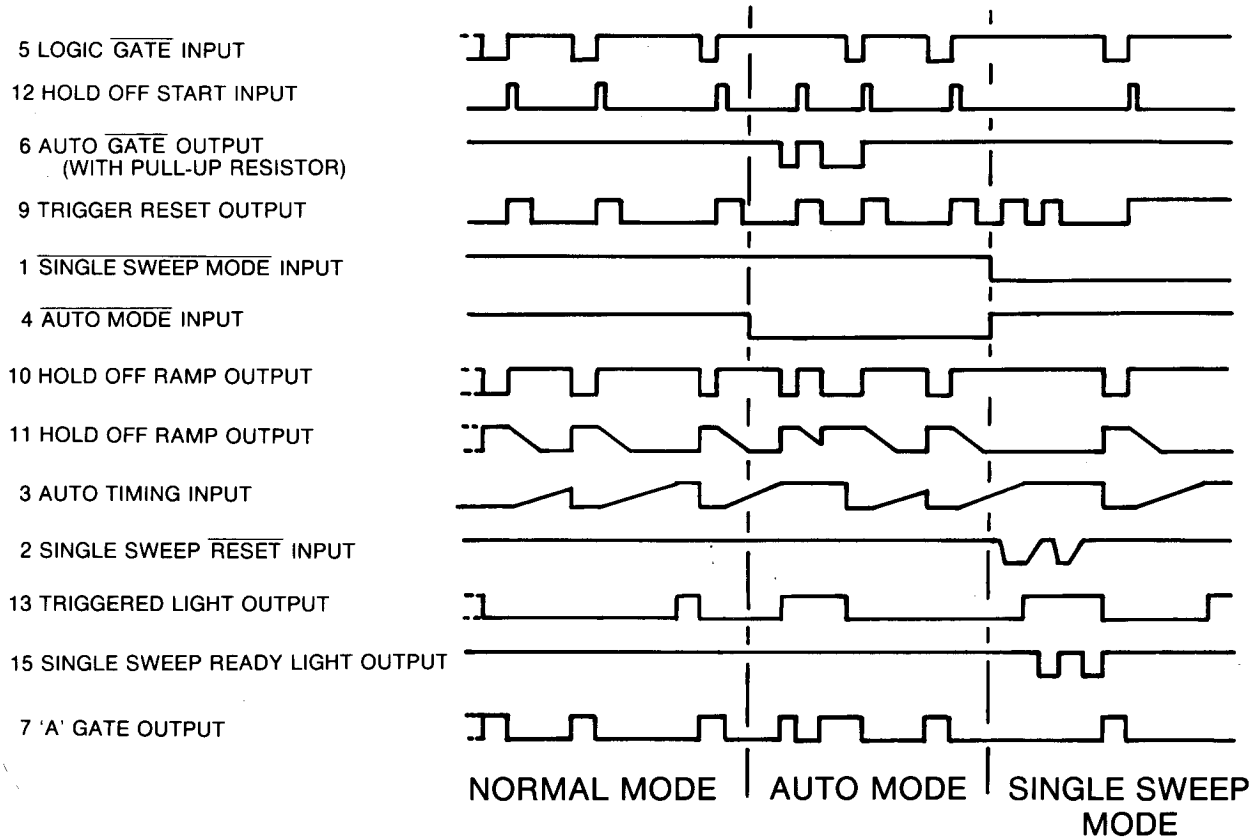


FIGURE 2



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SWEEP GENERATOR AND DELAY PICKOFF CIRCUIT

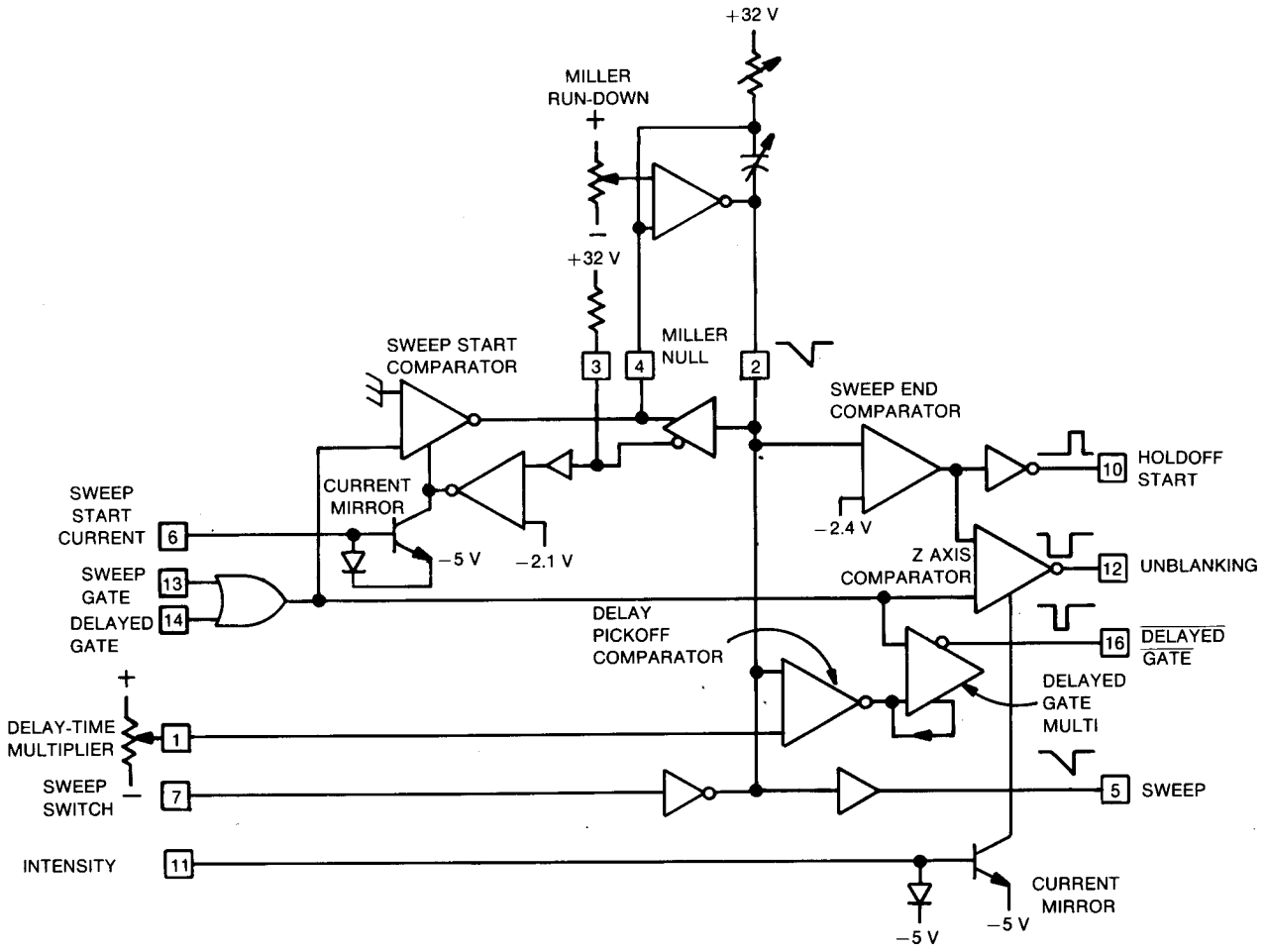
DESCRIPTION

The 155-0123-00 is a monolithic integrated sweep generator and delay pickoff circuit. It is used both as a delaying sweep and as a delayed sweep integrated circuit.

FEATURES

- Miller amplifier.
- Delay pickoff.
- Sweep start comparator.
- Sweep switch.
- Sweep end.
- Z axis circuits

BLOCK DIAGRAM



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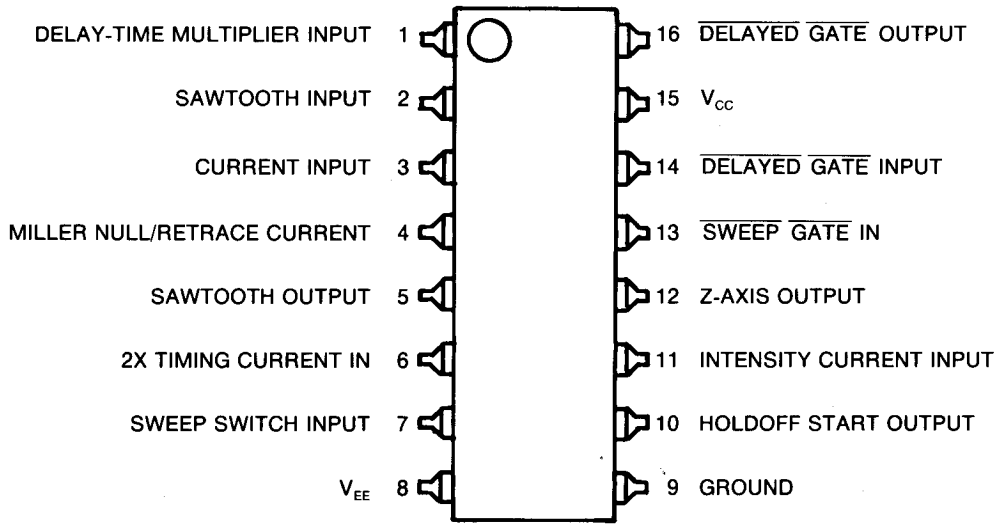
ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
	Input current* (Pins 6, 7, 11, 13)	10	mA
V_{CC}	(Pin 15)	+7.5	V
V_{EE}	(Pin 8)	−7.5	V
T_{STG}	Storage temperature range	−55 to 125	°C
	Operating IC ambient temperature range	−15 to +85	°C
P_D	Maximum power dissipation	335	mW
T_j	Maximum junction temperature	125	°C
	Maximum output current (Pin 7 low) (Pin 5)	4.0	mA

***These inputs are to one or more junctions to one of the supplies. Any applied voltage must be current limited.**

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN	MAX	UNITS
I_{CC} Supply Current (Pin 15)	15	35	mA
V_{EE} Supply Voltage (Pin 8)	−5.25	−4.75	V
I_{EE} Supply Current (Pin 8)	−50	−25	mA
Delay Time Input Bias Current (Pin 1) $V_{IN} = V_{pin\ 2} + 1$ volt	0	2	μA
Delay Time Input Voltage Range (Pin 1)	−5	+5	V
Output Voltage (Pin 10, open) (See note 1) Pin 2 ground (Pin 10)	4	5	V
Output Voltage (Pin 10, open) Low State, Pin 2 ground (Pin 10)	−.9	−.6	V
Hold-off Start Output Current During Sweep (V_{pin} + 5 V) (Pin 10)	1.5	2.75	mA
Retrace Current During Hold-off Pin 4 = 2 V (Pin 4)	1.16	2.3	mA
Retrace Current During Sweep (See Note 2) Pin 4 = 2 V (Pin 4)	2.25	3.75	mA
Leakage Retrace Current Pin 4 = 2 V (Pin 4)	−15	+15	mA
Delay Gate Output Voltage Pin 1 > 1 Volt (Pin 16)	−200	+200	mA
Delay Gate Output Voltage Pin 1 < 1 Volt (Pin 16)	1.2	1.6	V

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ELECTRICAL CHARACTERISTICS (cont)

PARAMETER/CONDITIONS	MIN	MAX	UNITS
Delay Gate Output Voltage Pin 1 > 1 V Pin 16 voltages = .6 V (Pin 16)	1.68	3.92	mA
Miller Output Bias Current Pin 2 = 0 V (Pin 2)	2.7	5	mA
Miller Output Bias Voltage (Pin 2)	4	5.3	V
Sweep Output Voltage Low, Pin 7 = HI (Pin 5)	−5	−4	V
Sweep Output Voltage High (peak to peak) Pin 7 = Low (Pin 5)	4	5.3	V
Sweep Output Current Pin 7 = HI (Pin 5)	2.94	3.74	mA
Sweep Output Peak Voltage Above Ground (Pin 5)	1.7	2.5	V
Constant Current Source Measurement Pin 3, with 4.7 MΩ Resistor to 32 Volts (Pin 3)	1.5	3.5	V
Unblanking Current Pin 14 = Low (See Notes 3, 4) Pin 11 Force 2 mA at −2.6 V (Pin 12)	1.6	2.4	mA
Unblanking Current Pin 14 = High (See Notes 3, 4) Pin 1 Force 5 mA at −2.6 V (Pin 12)	1.9	6.0	mA
Input Voltage (Sweep Run) (Pins 13, 14)	0.0	0.3	V
Input Voltage (Sweep Off) (Pins 13, 14)	1.0	1.4	V
Input Bias Current (Pins 13 or 14 = 1 Volt) (Pins 13 or 14)	0.0	50.0	μA

ELECTRICAL CHARACTERISTICS (Note Section)

Note 1: Pin 10 goes positive at the end of Sweep to start Hold-off.

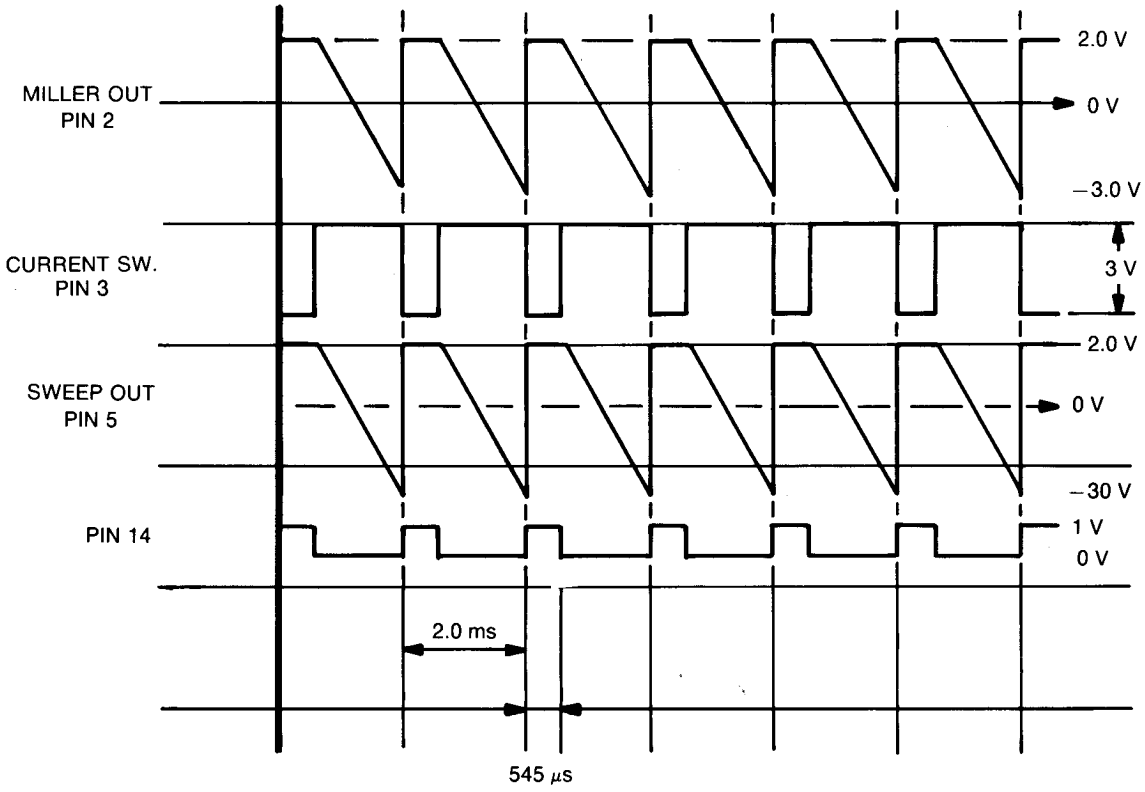
Note 2: Retrace Current is 3 mA ± 20% plus 1/2 of Start Level (Pin 6) Current ± 20%. After Retrace, and during Hold-off, Current is 1/2 of Start Level Current ± 20%.

Note 3: 0 to 3 mA is the normal Unblanking Current. 3 to 6 mA overrides Blanking for XY operation.

Note 4: Pin 12 Normal Operation Current = Pin 11 Current ± 25% from 0 mA to 3 mA when in normal operation plus twice the current of any Pin 11 Current over 3 mA ± 25%.

Pin 12 X-Y Override Condition Current = Pin 11 Current ± 25% minus 3 mA in the X-Y Override Condition.

WAVEFORMS



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APPLICATIONS INFORMATION

PRODUCT PRECAUTIONS

Input Protection

Input current, Pins 6, 7, 11, 13, and 14 less than 10 mA. Negative applied voltage must be greater than −5 Volts.

Output Loading

Load on Pin 5, while in High State, less than 4 mA (High State).

Power Supply Turn-On/Turn-Off Sequence

Turn "on" sequence:

First ..... −5 Volt Supply
Second ..... +5 Volt Supply

Turn "off" sequence:

First ..... +5 Volt Supply
Second ..... −5 Volt Supply

RELIABILITY

λ, failure rate $\leq$ .02%/1K hours at 75°C tj.
Thermal resistance junction to case 87°C/W.

5

HORIZONTAL PREAMPLIFIER

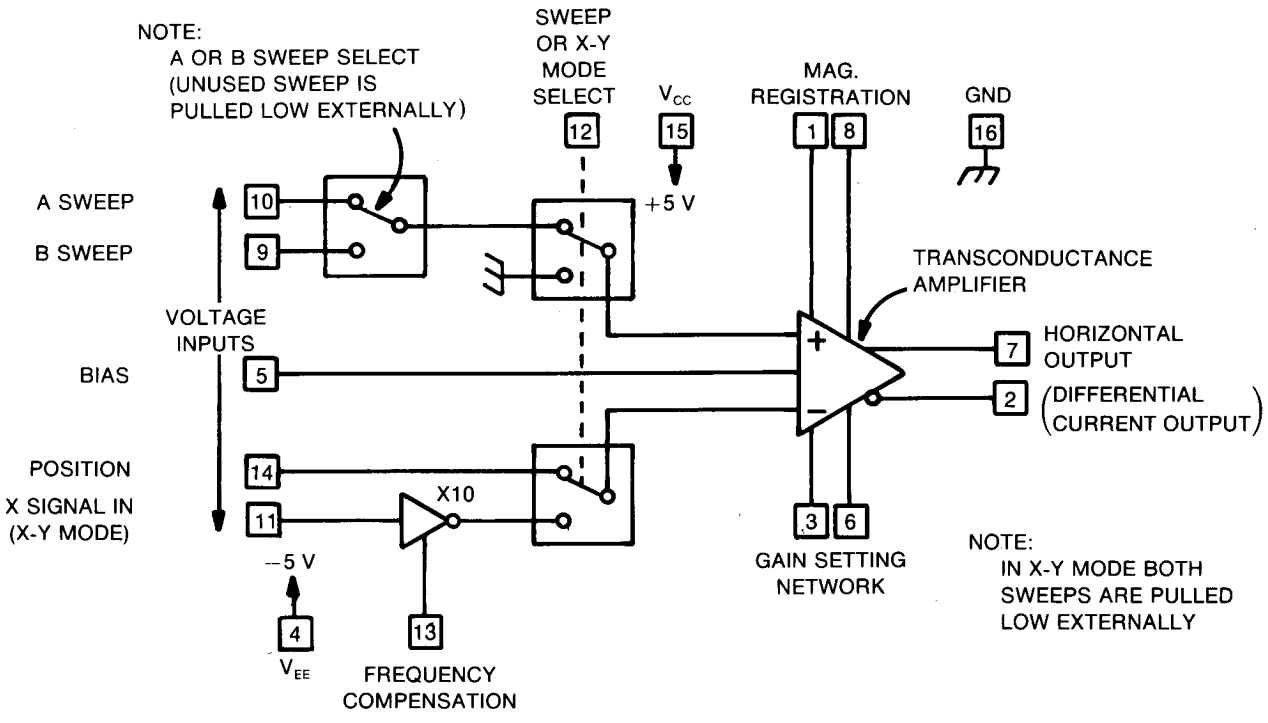
DESCRIPTION

The 155-0124-00 is a monolithic integrated horizontal preamplifier designed to accept single-ended input signals from A sweep, B sweep, horizontal position, X-Y mode and X-input. The output of a 155-0124-00 is a differential current which drives an external horizontal output amplifier.

FEATURES

- Switching between A sweep and B sweep is done internally.
- Switching between the sweep mode and the X-Y mode is done internally.
- An internal preamplifier amplifies the X signal from a vertical channel by a factor of 10. Bandwidth of X preamp is greater than 5 MHz.
- Power dissipation (typical application) = 185 mW in sweep mode and 215 mW in X-Y mode.
- Operates from +5 volt and −5 volt supplies

BLOCK DIAGRAM



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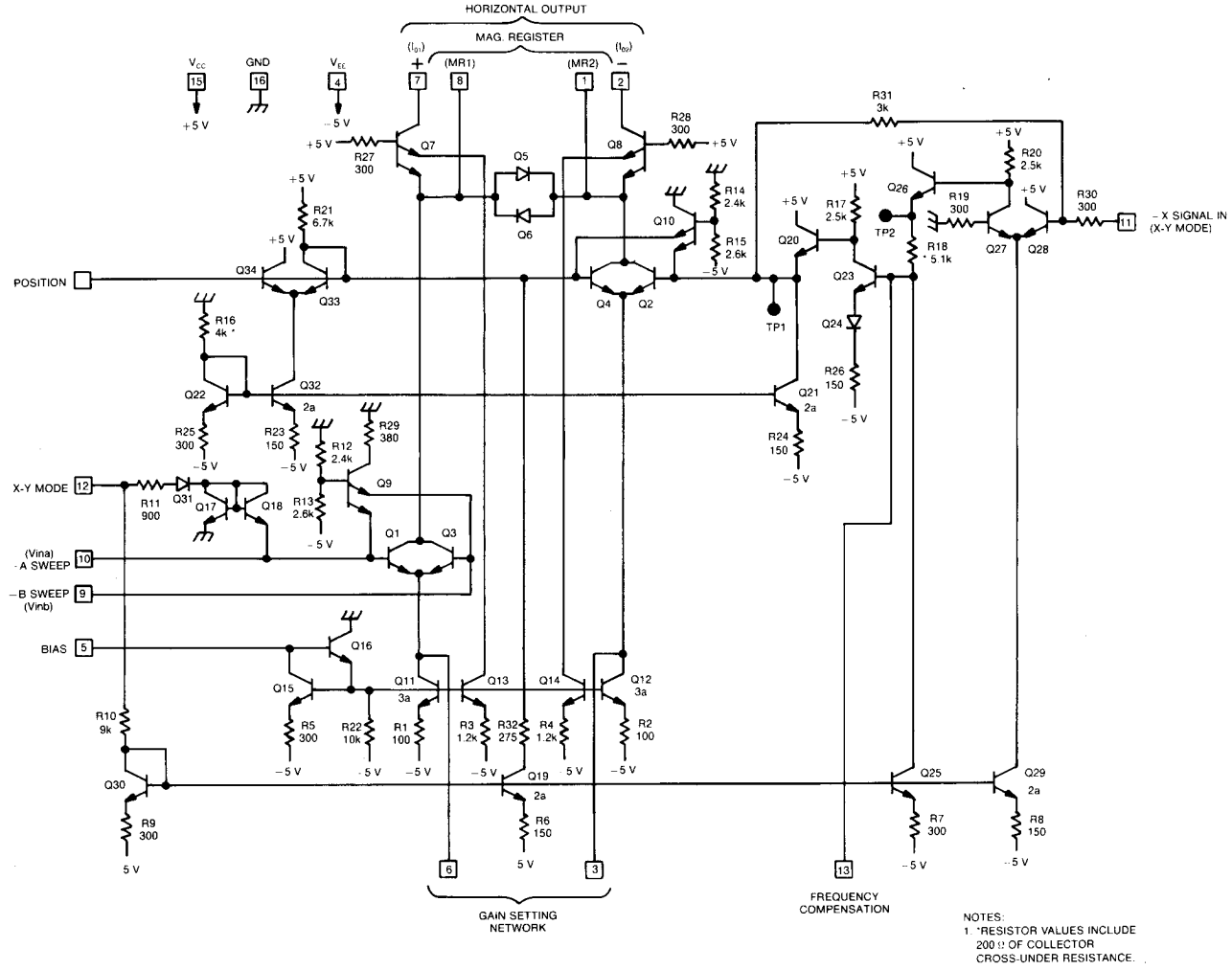
HORIZONTAL OUTPUT
MAG. REGISTER
(MR1)
(MR2)
V_{CC}
GND
V_{EE}
+5 V
−5 V
R27 300
R28 300
R31 3k
R21 6.7k
R14 2.4k
R15 2.6k
R20 2.5k
R17 2.5k
R19 300
R30 300
R18 5.1k
R16 4k
R25 300
R23 150
R12 2.4k
R29 380
R26 150
R24 150
R11 900
R13 2.6k
R10 9k
R5 300
R22 10k
R1 100
R3 1.2k
R32 275
R4 1.2k
R2 100
R9 300
R6 150
R7 300
R8 150
Q5
Q6
Q7
Q8
Q10
Q20
Q23
Q24
Q26
Q27
Q28
Q4
Q2
Q34
Q33
Q32
Q22
Q21
Q31
Q17
Q18
Q9
Q1
Q3
Q16
Q15
Q11
Q13
Q14
Q12
Q30
Q19
Q25
Q29
TP1
TP2
POSITION
X-Y MODE
(Vina) -A SWEEP
−B SWEEP (Vinb)
BIAS
− X SIGNAL IN (X-Y MODE)
GAIN SETTING NETWORK
FREQUENCY COMPENSATION
NOTES:
1. *RESISTOR VALUES INCLUDE 200 Ω OF COLLECTOR CROSS-UNDER RESISTANCE.

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	VALUES	UNITS
V_{CC}	(Pin 15)	Ground to 5.5	V
V_{EE}	(Pin 4)	Ground to −5.5	V
	Sweep input voltage (Pins 9 and 10)	+2.4 to −2.6	V
	I-source reference (Pin 5)	5.0	mA
	X-input	+.24 to −.24	V
	MGF (Magnified) register current (Pins 1 and 8)	3 times I-source	
T_{SG}	Storage temperature	−55 to 125	°C
T_A	Operating ambient temperature	+85	°C
P_D	Max power dissipation	235	mW
T_j	Max junction temperature	125	°C

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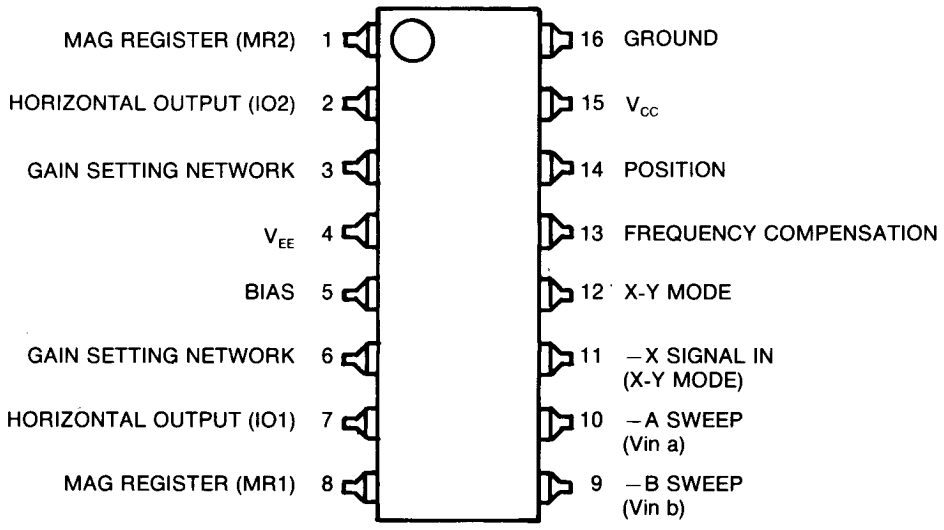
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	MAX	UNITS
Average Output Level (Test Setup Note #1)	2.17	2.57	mA
Differential Output Level (Test Setup Note #2)	−0.3	+ 0.3	mA
A to B Input Offset (Test Setup Notes #3, 4)	−0.1	+0.1	mA
A to X Input Offset (Test Setup Notes #3, 5)	−0.2	+0.2	mA
X Transconductance (Test Setup Note #6)	4.5		mMHOS/SIDE
A_{in} Transconductance (Test Setup Note #7)	5.0		mMHOS/SIDE
B_{in} Transconductance (Test Setup Note #8)	5.0		mMHOS/SIDE
B_{in} Risetime (Test Setup Note #9)		25.0	nS
A_{in} Risetime (Test Setup Note #10)		25.0	nS
X_{in} Risetime (Test Setup Note #11)		100	nS
Range (Differential) (Test Setup Note #12)	−2.4	+2.4	mA (Differential)
Range (Horizontal Position) (Test Setup Note #13)	−2.4	+2.4	mA (Differential)

ELECTRICAL CHARACTERISTICS (cont)

Test Set Up Notes

	POSITIONS		
SW-1	SW-2	SW-3	(Note #1)
Gain	X/Y	A* Sweep	TEST #1 is done to insure that the CRT Average Plate Volts will be 48 V ±4 V (CRT Spec).This limit will be reached if $\frac{(I_{01} + I_{02})}{2} = 2.37 \pm .225$ mA.
2	1	1	
X1* 2	A Sweep* 1	1	(Note #2) TEST #2 is done to insure that the MAG. REGISTER has enough range. This limit will be reached if $I_{01} - I_{02} = \pm .1$ mA.
XI0* 1	A Sweep* 1	1	(Note #3) TEST #3 is done to establish a reference for TESTS #4 and #5. Measure $\lvert I_{01} - I_{02} \rvert$ = A offset.
Gain* X10 1	B Sweep* 1	1	(Note #4) TEST #4 is done to measure A/B offset. $I_{01} - I_{02}$ = B offset $\lvert A - B \rvert = \leqslant .1$ mA.
Gain* 2	X* Amp 50 Ω Term. No Sig. 2	3	(Note #5) TEST #5 is done to measure A/X offset. $\lvert I_{01} - I_{02} \rvert$ = A − X = ± .2 mA
Gain* X1 2	X Amp. 2	3	(Note #6) TEST #6 is done to measure X Amplifier Gain. a) Measure $I_{01} - I_{02}$, no signal in. Apply 100 mV DC to X Input. b) Measure $I_{01} - I_{02}$ c) $\lvert a - b \rvert \geqslant 1$ mA
Gain* X10 1	A* Sweep 1	1	(Note #7) TEST #7 is done to measure A Sweep Gain. a) Measure $I_{01} - I_{02}$, no signal in. b) Apply 100 mV DC to A_{input}, measure $I_{01} - I_{02}$. c) $\lvert a - b \rvert \geqslant 1$ mA
Gain* X10 1	A* Sweep 1	2	(Note #8) TEST #8 is done to measure B Sweep Gain. a) Measure $I_{01} - I_{02}$, no signal in. b) Apply 100 mV DC to B input. Measure $I_{01} - I_{02}$. c) $\lvert a - b \rvert \geqslant 1$ mA
Gain X10* 1	B Sweep* 1	2	(Note #9) TEST #9 is done to measure B_{in} Risetime. a) Apply fast rise pulse (106 Tek Squarewave Generator "example"). t_p B in b) Measure t_r and t_f of I_{01} and I_{02}. t_r and $t_f \leqslant 25$ nSEC.

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ELECTRICAL CHARACTERISTICS (cont)

Test Set Up Notes			
Gain* X10 1	B* Sweep* 1	1	(Note #10) TEST #10 is done to measure A_{in} Risetime. a) Apply fast rise pulse (Tek 106) to A_{in} b) Measure t_r and t_f of I_{01} and I_{02}. t_r and $t_f \leq$ 25 nSEC.
Gain* X1 2	X in* 2	3	(Note #11) TEST #11 is done to measure X_{in} Risetime. a) Apply fast rise pulse (Tek 106) to X_{in} b) Measure t_r and t_f of I_{01} and I_{02}. t_r and $t_f \leq$ 100 nSEC.
Gain* X1 2	X_{in}* 2	3	(Note #12) TEST #12 is done to measure Range of the I.C. a) Apply +300 mV DC to X_{in} $I_{01} \geq$ 3.57 mA $I_{02} \leq$ 1.17 mA b) Apply −300 mV DC to X_{in} $I_{01} \leq$ 1.17 mA $I_{02} \geq$ 3.57 mA
2	1	1	(Note #13) TEST #13 is done to measure Position Input Range. a) Apply +2.5 V to Position Input $I_{02} \geq$ 3.57 mA $I_{01} \leq$ 1.17 mA b) Apply −2.4 V to Position Input $I_{02} \leq$ 1.17 mA $I_{01} \geq$ 3.57 mA

*** The Function of that Switch Position.**

5

RELIABILITY

λ failure rate $\leq$ .02%/1K hours at 75°C Tj

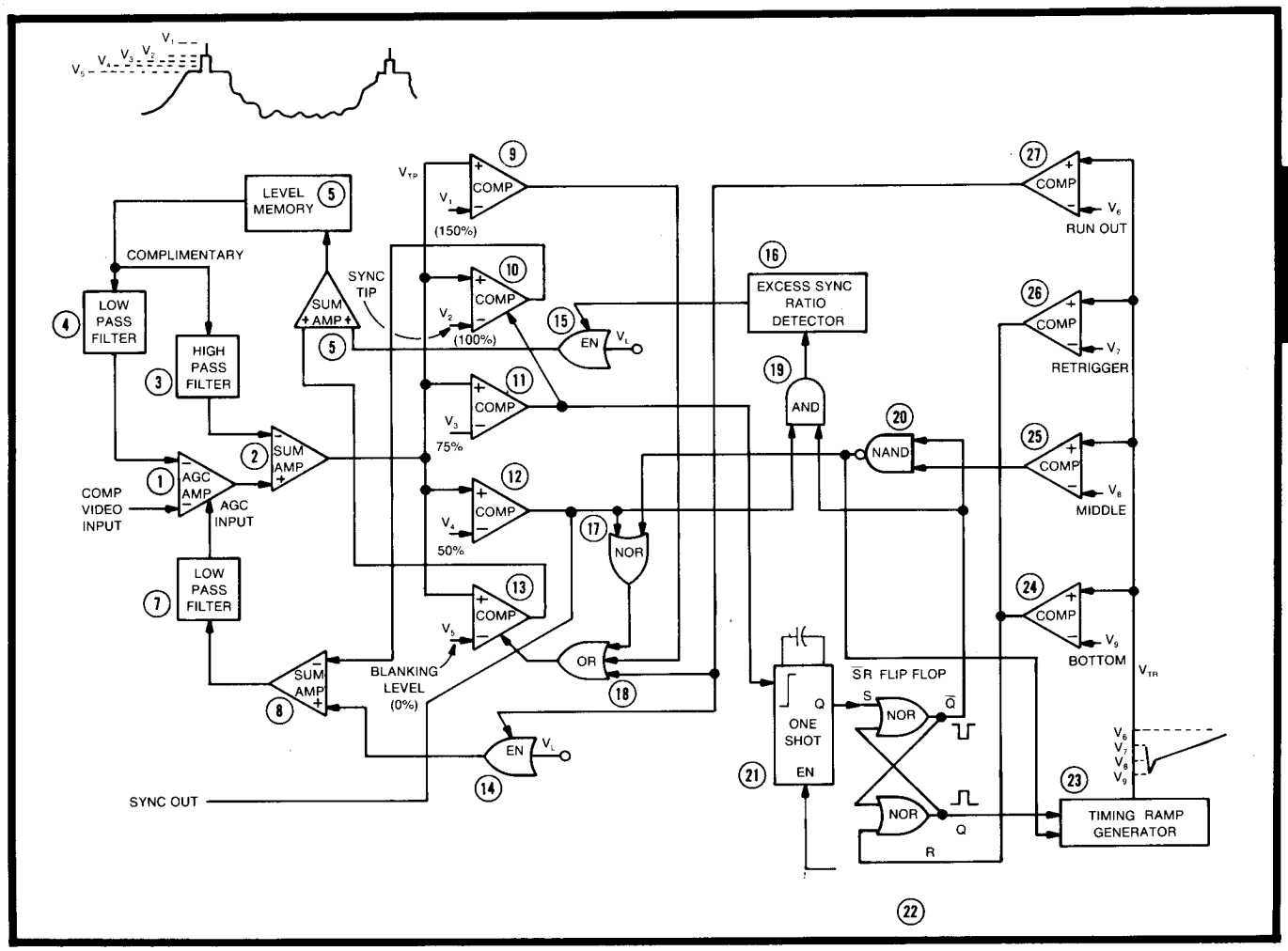
SYNC STRIP CIRCUIT

DESCRIPTION

The 155-0144-00 generates an output pulse whose leading edge reproduces the timing of the 50% point on the leading edge of the sync pulses contained in a composite video waveform.

FEATURES

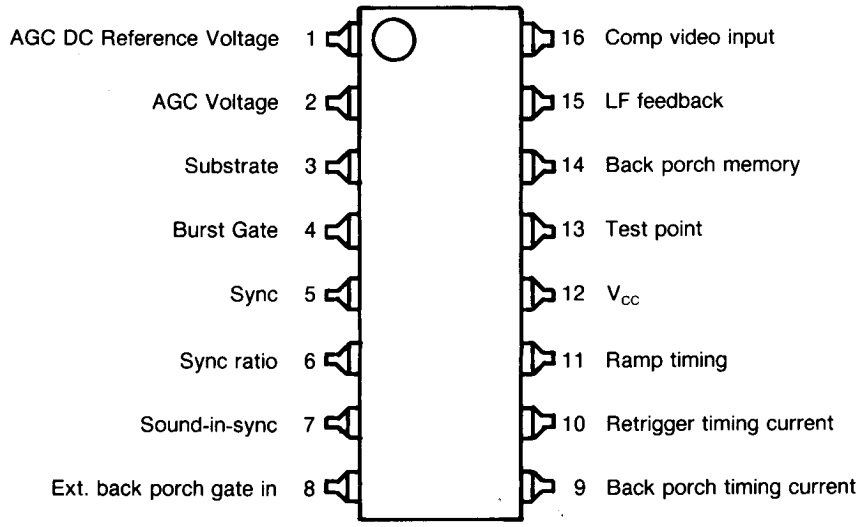
- Open collector outputs: Comp sync, sound-in-sync, and back porch gate.
- AGC is based upon input sync amplitude. A "test point" is available with inverted comp video reference to 0.8 V sync amplitude.
- Wide input dynamic range with leading sync edge timing preserved.
- Provides a block sync output to be used with sound-in-sync video input.
- Provides a back porch gate suitable for video clamping amplifiers.
- Internal timing, adjustable by external components to accommodate different line rates, creates a window for the acceptance of sync inputs. (This minimizes sensitivity to noise bursts.)
- The gain for the input amplifier (and thus the amplitude of the input sync) can be determined between the AGC voltage and the AGC reference pins.



ABSOLUTE MAXIMUMS

SYMBOL	IDENTIFICATIONS	VALUES	UNITS
	Input Current (Pin 16)	±2	mA
V_{CC}	(Pin 12)	+16	V
	Back Porch Gate Output (Pin 4)	−4	mA
	Output Voltage (Pins 4, 5, 7)	+10	V
	Maximum operating temperature (Results in a 125°C Junction temperature)	80	°C
	Power Dissipation	400	mW

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS*

SYMBOL	PARAMETER/CONDITIONS	MIN	MAX	UNITS
V_{TP}	Test Point Voltage (Pin 13)	11.0	13.0	V
V_{SY}	Sync Out Voltage (Pin 5)	4.9	5.1	V
V_{BP}	Back porch Gate Out Voltage (Pin 4)	4.9	5.1	V
V_{SS}	Sound in syncs out voltage (Pin 7)	4.9	5.1	V
V_{RP}	Ramp timing voltage (Pin 11)	13.6	14.6	V
V_{AGC}	AGC Voltage (Pin 2)	1.8	2.6	V
V_{REF}	AGC Reference Voltage (Pin 1)	3.3	3.9	V
V_{SR}	Sync Ratio Voltage (Pin 6)	12.0	14.0	V
$V_{BP(IN)}$	Back Porch Gate In Voltage (Pin 8)	9.5	11.5	V
V_{IN}	Input Voltage (Pin 16)	1.8	2.4	V
V_{LF}	LF Feedback Voltage (Pin 15)	7.0	9.0	V
V_{MEM}	Back Porch Memory Voltage (Pin 14)	8.0	10.0	V
V_{RT}	Retrigger Input Voltage (Pin 10)	0.6	0.8	V
V_{BPT}	Back Porch Timing Voltage (Pin 9)	0.8	1.4	V
T_{IO}	Input to Output Delay (V_{gen} to Pin 5) (Figure 1) V_{gen} = 286 mV of horizontal Sync. Between 50% points	120		nS
V_{LO}	Output logic zero levels (Pins 4, 5, 7) (Figure 1)	300	750	mV
T_X	Trailing edge of test point pulse to leading edge of back porch gate output pulse (Pin 13 to Pin 4) (Figure 1)	100	250	nS

***V_{gen} = 0 volts unless otherwise noted.**

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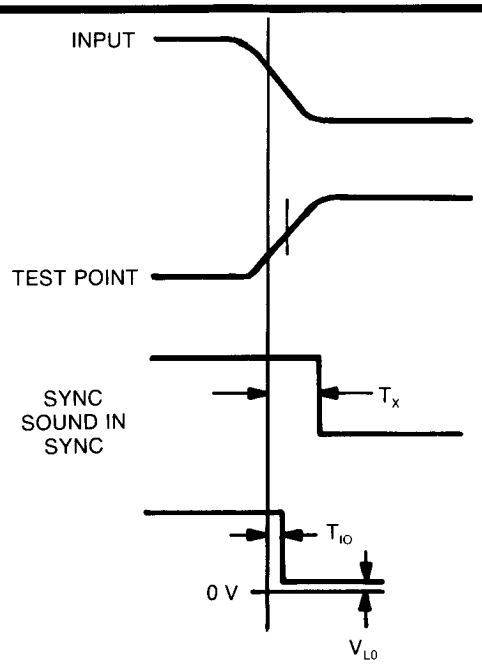
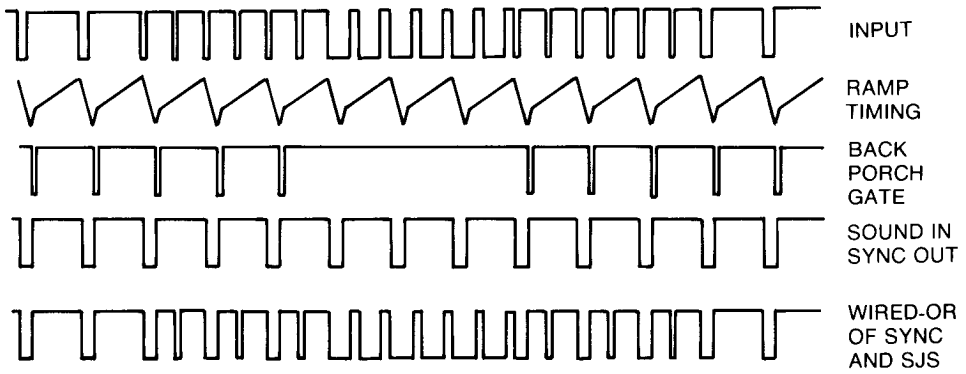
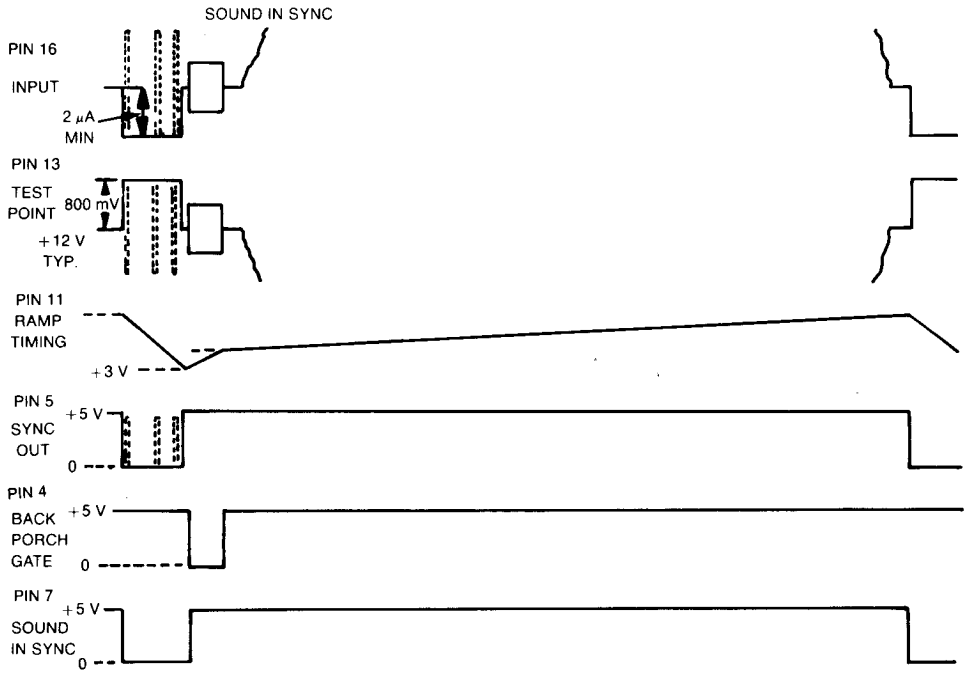
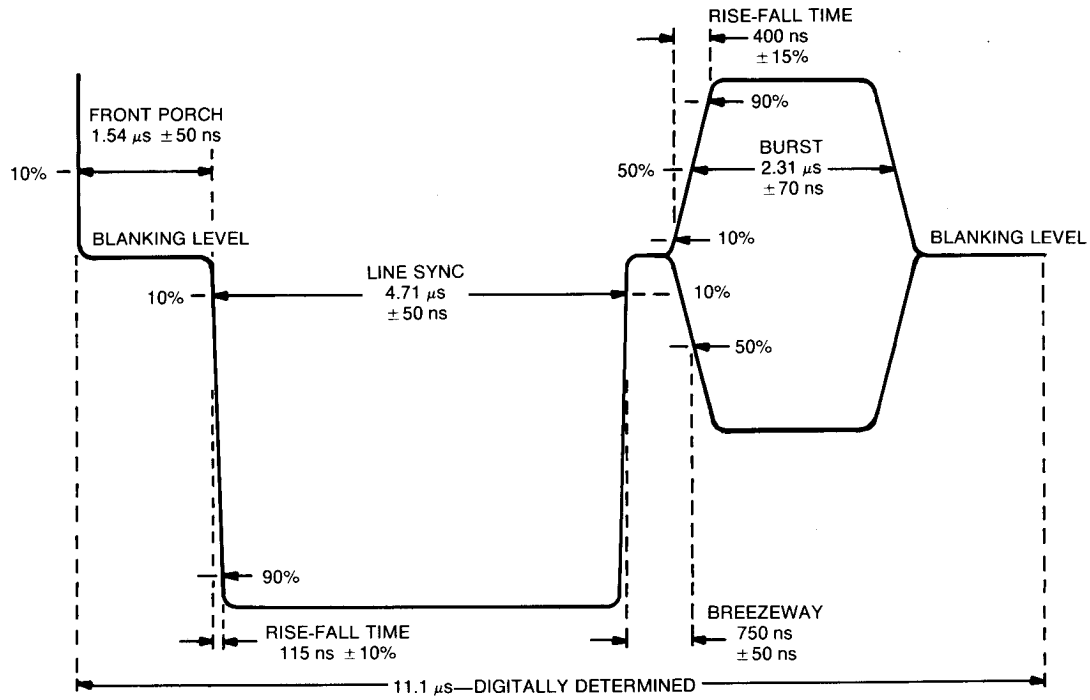


INPUT AND OUTPUT WAVEFORMS

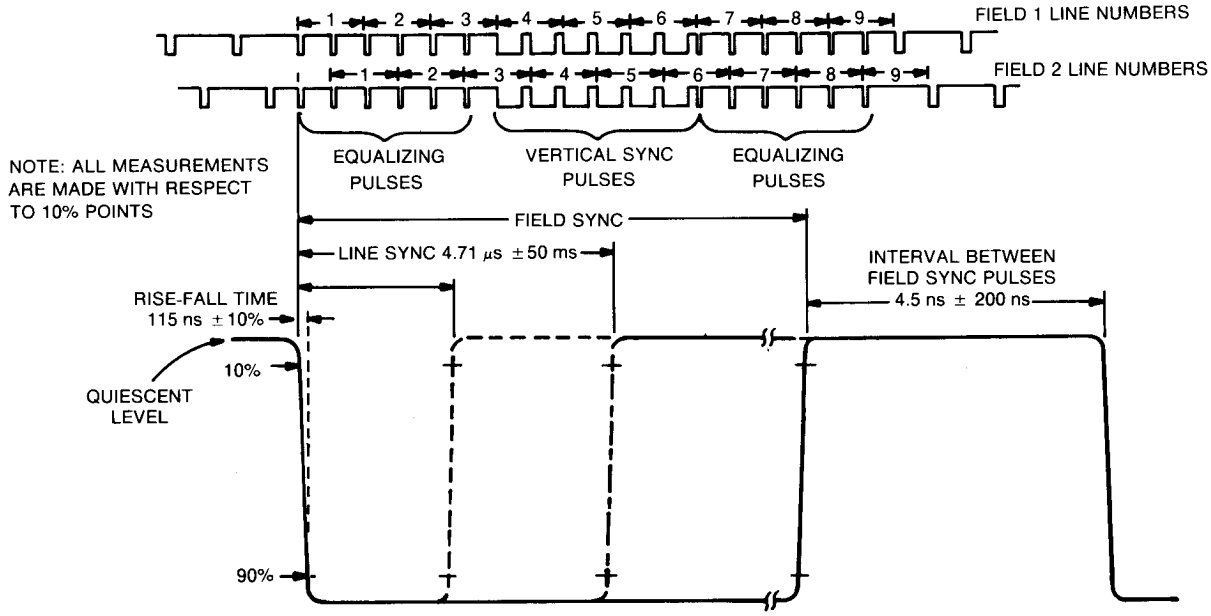




COMP VIDEO HORIZONTAL BLANKING



COMP SYNC BLANKING



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RELIABILITY

λ failure rate $\leq$ .02%/1K hours at 75°C Tj

PULSE OUTPUT AMPLIFIER

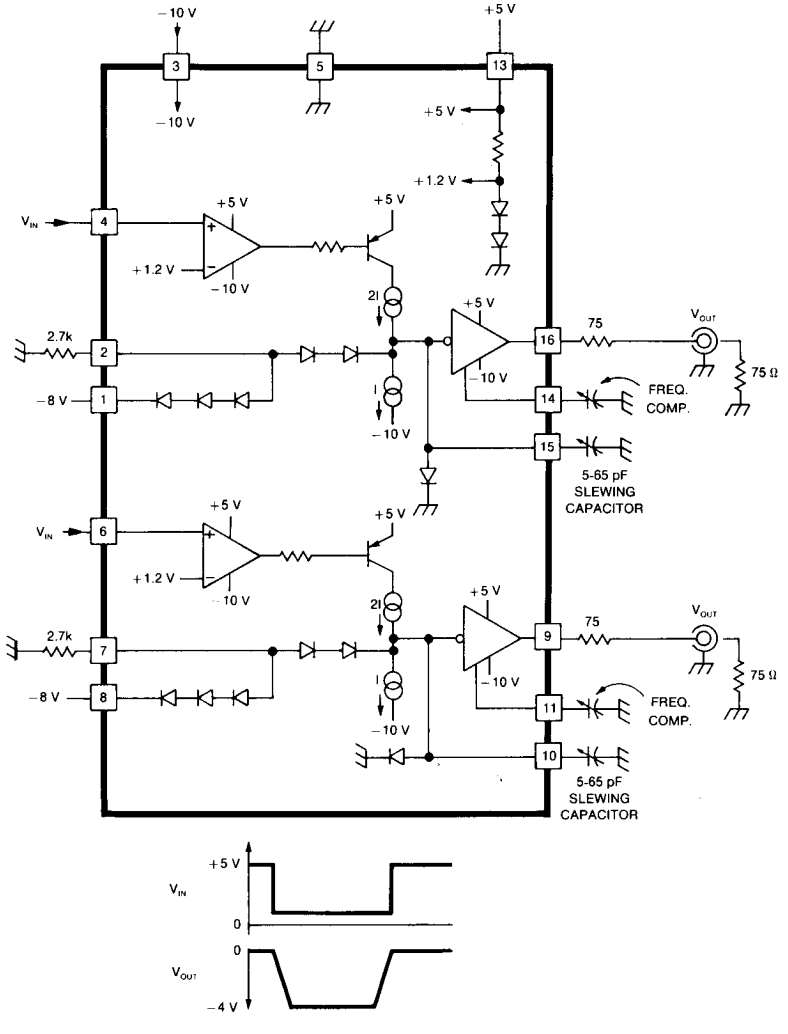
DESCRIPTION

The 155-0145-00 provides a controlled risetime output pulse occurring between ground and a programmable negative level, given a TTL input pulse. Two such amplifiers are provided per package.

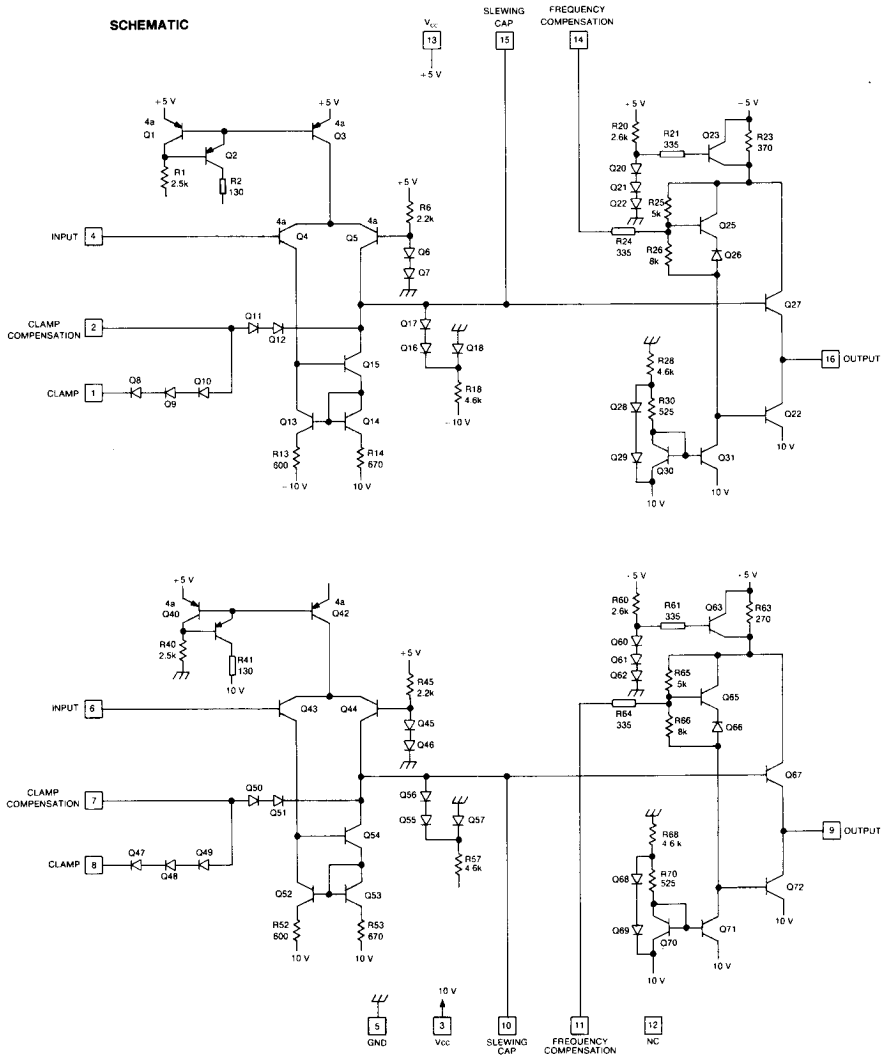
FEATURES

- 2 independent amplifiers
- Controlled and matched rise and falltimes, selectable by external capacitor
- TTL compatible inputs
- Output voltage swings from 0 to −8 volts

BLOCK DIAGRAM



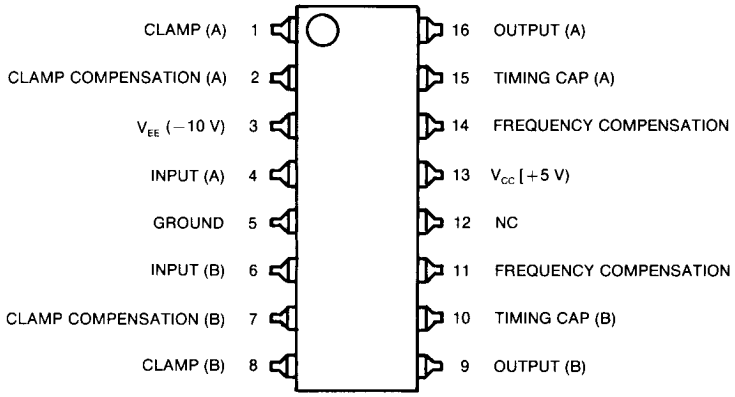
SCHEMATIC



ABSOLUTE MAXIMUMS

Input Voltage (Pins 4 and 6)	-4.5 V to V_{CC}
Output Sink Current (Pins 9 and 16)	150 mA
Output Source Current (Pins 9 and 16)	30 mA (Under Controlled Conditions)
V_{CC} (Pin 13)	$+5.25$ Volts
V_{EE} (Pin 3)	-10.25 Volts
Operting Ambient Temperature	0°C - 50°C
Maximum Power Dissipation	550 mW at 50°C
Input Voltage (Pins 2 and 7)	2.0 V to -6.0 Volts
Input Voltage (Pins 1 and 8)	$V_{pins\ 2\ and\ 7}$ at -2.4 Volts
Maximum Die Temperature	$+125$°C

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Logical "0" Voltage	Pins 4, 6		0.8	V
Input Logical "1" Voltage	Pins 4, 6	2.5		V
Input Current (For V_{IN} = 2.5 Volts)	Pins 4, 6		500	μA
Charging Current (NOTE 1)	Pins 10, 15	800		μA
Risetime (NOTE 2)	Pins 9, 16	100		nS
Upper Output Clamp Voltage	Pins 9, 16	−0.1	+0.1	V
Lower Output Voltage Differential	$V_{Pin\ 9} - V_{Pin\ 8}$ $V_{Pin\ 16} - V_{Pin\ 1}$	−0.1	+0.1	V

NOTES: 1. Minimum current into or out of pin under static conditions

2. For output loaded with 150 Ω from pin to ground and slewing capacitor of 2 pF.

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Reliability

λ, failure rate ≤.02%/1K hours at 75°C Tj

Thermal resistance, θ_{ja} 107.4°C/W

GEOMETRY & FOCUS CORRECTION

DESCRIPTION

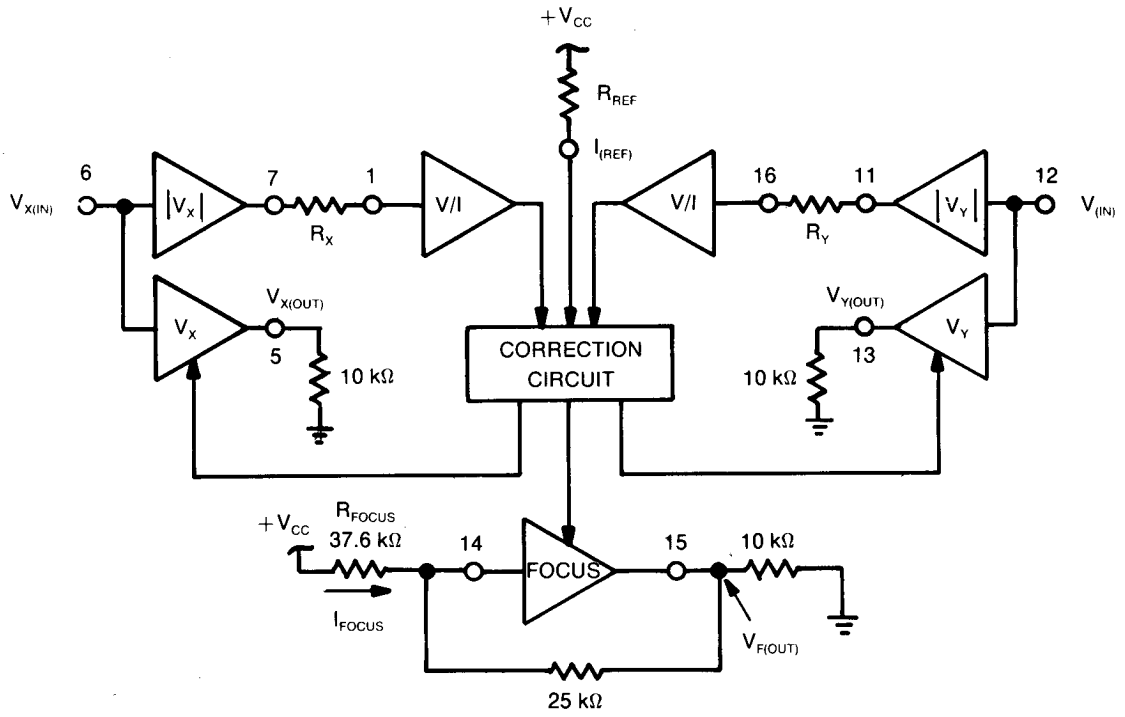
The 155-0152-01 is a CRT Geometry and Focus Correction Integrated Circuit. It contains two Pre-Amplifiers (for X and Y Axis), whose nonlinear transfer functions compensate for the pin-cushion distortion seen on CRT displays with electromagnetic deflection systems. The amount of correction is set by external resistors. A third amplifier generates an error signal which can be used to correct for defocusing due to spot position on the CRT.

*FEATURES

- Positional Accuracy: Better than ±1% relative to screen diagonal.
- Linearity: Better than ±1% deviation relative to length of line.
- Vector Length Accuracy: Better than ±2% relative to the vector length.
- Speed: Corner to corner jump and settle to 1% in 10 μs.

***As seen on the 4006-1 Display Terminal with 10", 60° CRT.**

BLOCK DIAGRAM



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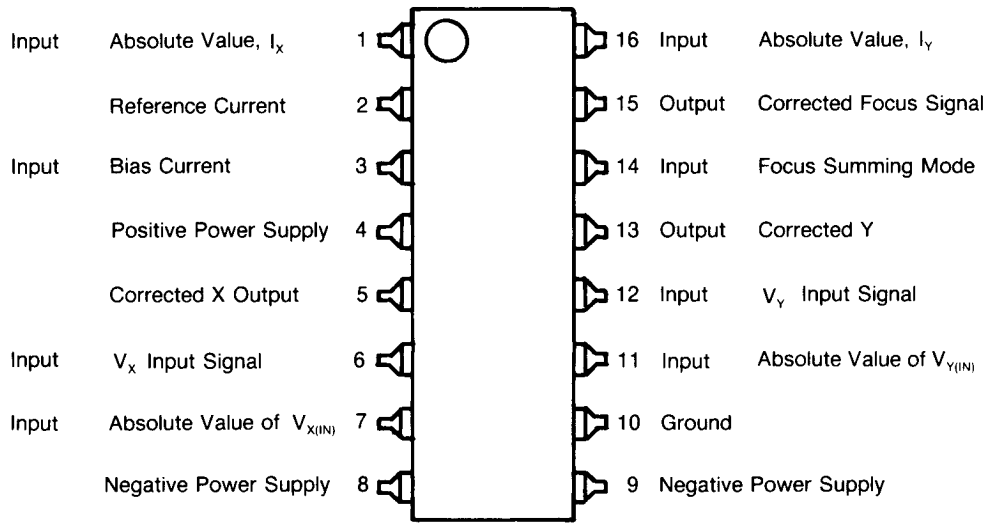
ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUES
	Power Supply Voltage	± 15 V
	Input Voltage	± 5.0 V
T_{SG}	Storage Temperature	−55°C to +125°C
T_A	Operating Ambient Temperature	+70°C
P_D	Maximum Power Dissipation	540 mW
T_J	Maximum Junction Temperature	+125°C
R_L	Minimum Load Resistance	5 KΩ
C_L	Maximum Load Capacitance	10 pF

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

Symbol	Parameter*	Conditions	Min	Max	Units
I_{CC}	V_{CC} Supply Current	Note 1	10	18	mA
I_{EE}	V_{EE} Supply Current	Note 1	−18	−12	mA
I_{GND}	Ground Current	Note 1	0	2	mA
A_V	Amplifier Voltage Gain	Notes 2, 4	0.9	1.1	
$V_{(OFFSET)}$	Output Offset Voltage	Notes 1, 3	−300	+300	mV
$A_{V(ABS)}$	Absolute Value Amp. Gain	Notes 1, 8	0.95	+1.05	
$V_{ABS(OFFSET)}$	Absolute Value Amp. Offset	Notes 1, 3	10	+300	mV
$V_{CORNER(AVG)}$	Average Corner Vector Voltage	Notes 1, 5	4.54	5.54	V
$V_{CORNER(DEV)}$	Corner Vector Voltage Deviation	Notes 1, 5		5	%
$V_{ON\text{-}AXIS\ (ERROR)}$	On-Axis Vector Voltage Error	Notes 1, 5, 6		2	%
$V_{ON\text{-}AXIS\ (DEV)}$	On-Axis Vector Voltage Deviation	Notes 1, 5, 6		6	%
$V_{F(AVG)}$	Average Focus Voltage	Notes 1, 7	3.60	4.70	V
$V_{F(OFFSET)}$	Focus Offset Voltage	Notes 1, 3	−500	+500	mV
$V_{F(DEV)}$	Focus Offset Deviation	Notes 1, 7		10	%

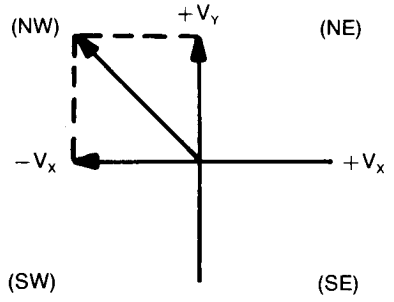
***PARAMETRIC DEFINITIONS**

V_{OUT} specifications subtract the Output Offset Voltage.

$$V_{OUT} = V_{OUT(Measured)} - V_{OUT(Offset)}$$

For simplicity, a geographic nomenclature will be used in locating X and Y Vectors.

Example: A "NW" (Northwest) Vector would be realized with a negative input on "X" and a positive input on "Y".



$$V_{CORNER} = \sqrt{V_{X(OUT)}^2 + V_{Y(OUT)}^2}$$

ELECTRICAL CHARACTERISTICS (cont)

R_{REF} and R_{BIAS} set Internal Bias Currents.

R_{BIAS} = 115.6 KΩ (V_{EE} = −12 V)
132.0 KΩ (V_{EE} = −15 V)

R_{REF} = 14.67 KΩ (V_{EE} = −12 V)
19.63 KΩ (V_{EE} = −15V)

R_{FOCUS} = 37.60 KΩ

R_{FOCUS} is chosen so that V_{FOCUS} = 0 V when $V_{IN(X)}$ and $V_{IN(Y)}$ have values corresponding to the corner of the display.

R_X and R_Y are used to set currents to the voltage-to-current converters. All specifications are within 6 KΩ resistors unless otherwise noted. This value will vary with the individual application, and the amount of correction desired.

ELECTRICAL CHARACTERISTICS (Note Section)

NOTE 1

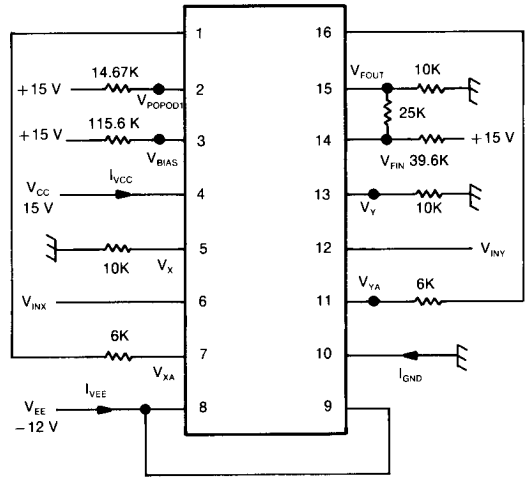
V_{CC} = +15 V

V_{EE} = −12 V

R_{REF} = 14.67 Kohm

R_{BIAS} = 115.6 Kohm

T_J = +25°C
Test Circuit #1



NOTE 2

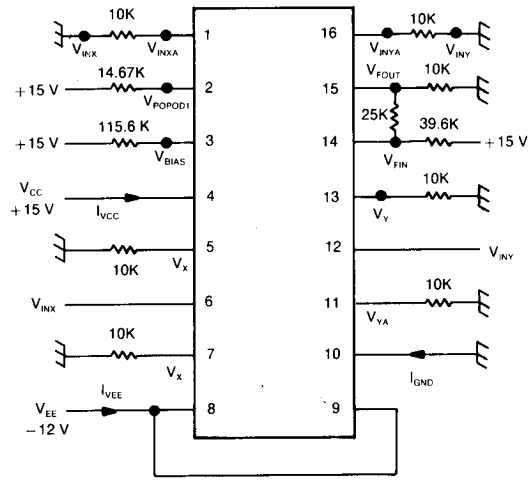
V_{CC} = +15 V

V_{EE} = −12 V

R_{REF} = 14.67 Kohm

R_{BIAS} = 115.6 Kohm

T_J = +25°C
Test Circuit #2



NOTE 3

Output Offset Voltages are measured with both inputs, $V_{X(IN)}$ and $V_{Y(IN)}$, at 0 V.

NOTE 4

Large Signal Voltage Gain of the X and Y Amplifiers, without Pin Cushion Correction.

V_{IN} = ± 5 V

$A_V = \frac{\Delta V_{OUT}}{10\ V}$

ELECTRICAL CHARACTERISTICS (Note Section cont)

NOTE 5

$V_{CORNER(AVG)}$ is the average of the four corner Vector Voltages, generated with ± 5 V inputs.

$$V_{CORNER(AVG)} = \frac{V_{NW} + V_{NE} + V_{SE} + V_{SW}}{4}$$

$V_{CORNER(DEVIATION)}$ defines the variation between the four V_{CORNER} voltages.

$$V_{CORNER(DEV)} = \frac{V_{CORNER(MAX)} - V_{CORNER(MIN)} \text{ X } 100}{V_{CORNER(AVG)}}$$

NOTE 6

$V_{ON\text{-}AXIS(AVG)}$ is the average of the Four Output Vector Voltages (V_N, V_S, V_E, V_W) as defined in the table below.

V_N $V_{IN(X)} = 0$ V $\quad V_{IN(Y)} = +5$ V
V_S $V_{IN(X)} = 0$ V $\quad V_{IN(Y)} = -5$ V
V_E $V_{IN(X)} = +5$ V $\quad V_{IN(Y)} = 0$ V
V_W $V_{IN(X)} = -5$ V $\quad V_{IN(Y)} = 0$ V

$$V_{ON\text{-}AXIS(AVG)} = \frac{V_N + V_S + V_E + V_W}{4}$$

$X_{ON\text{-}AXIS(ERROR)}$ is the percent difference between the $V_{ON\text{-}AXIS(AVG)}$ and the $V_{ON\text{-}AXIS(THEORY)}$, as calculated below.

$$V_{ON\text{-}AXIS(THEORY)} = \frac{5\sqrt{2}}{\sqrt{1 + \left(\frac{5\sqrt{2}}{V_{CORNER(AVG)}}\right)^2}}$$

$$V_{ON\text{-}AXIS(ERROR)} = \left(\frac{V_{ON\text{-}AXIS(AVG)} - V_{ON\text{-}AXIS(THEORY)}}{V_{ON\text{-}AXIS(THEORY)}}\right) \text{X } 100$$

$V_{ON\text{-}AXIS(DEVIATION)}$ defines the variation between the four On-Axis Vector Voltages

$$V_{ON\text{-}AXIS(DEV)} = \frac{V_{ON\text{-}AXIS(MAX)} - V_{ON\text{-}AXIS(MIN)}}{V_{ON\text{-}AXIS(AVG)}} \text{ X } 100$$

NOTE 7

$V_{FOCUS(AVG)}$ is the average of the Four Focus Voltages, as generated by $V_{IN(X)}$ and $V_{IN(Y)}$ at ± 5 V.

$$V_{FOCUS(AVG)} = \frac{V_{F(NW)} + V_{F(NE)} + V_{F(SE)} + V_{F(SW)}}{4}$$

$V_{FOCUS(DEVIATION)}$ defines the variation between the four V_{FOCUS} Voltages.

$$V_{FOCUS(DEV)} = \frac{V_{FOCUS(MAX)} - V_{FOCUS(MIN)}}{V_{FOCUS(AVG)}} \text{ X } 100$$

NOTE 8

Large Signal Voltage Gain of the X and Y Absolute Value Amplifiers.

$V_{IN} = \pm 5$ V

$$A_{V(ABS)} = \frac{\Delta V_{(ABS)}}{10 \text{ V}}$$

5

APPLICATIONS INFORMATION

SYMBOL	PARAMETER/CONDITIONS	TYPICAL	VOLTS
$V_{REF]}$	$V_{Reference\text{-}Current]}$ Pin #2 See Note 1, Electrical Characteristics	−2.8	V
$V_{BIAS]}$	$V_{Bias\text{-}Current]}$ Pin #3 See Note 1, Electrical Characteristics	−8.4	V

If all errors are zero the functions generated by the IC are given below:

$$V_{X(OUT)} = \frac{V_{X(IN)}}{1 + \left(\frac{I_X}{I_{REF}}\right)^2 + \left(\frac{I_Y}{I_{REF}}\right)^2}$$

$$V_{Y(OUT)} = \frac{V_{Y(IN)}}{1 + \left(\frac{I_X}{I_{REF}}\right)^2 + \left(\frac{I_Y}{I_{REF}}\right)^2}$$

$$V_{F(OUT)} = I_{FOCUS} - \frac{I_{REF}}{3}\sqrt{1+\left(\frac{I_X}{I_{REF}}\right)^2 + \left(\frac{I_Y}{I_{REF}}\right)^2}$$

5

R_X and R_Y are external resistors that set I_X and I_Y

$I_X = |V_{X(IN)}|$

$I_Y = |V_{Y(IN)}|$

$R_{REF} = R_{FOCUS}$ are external resistors that set I_{REF} and I_{FOCUS}

Product Precautions

Input Protection

Do not apply signals of greater than 5.0 V on either input $-V_X$ or V_Y.

Output Loading

WARNING

*Output capacitance is to be limited to a **maximum** of 10 pF on all outputs to avoid oscillation.*

Do not short outputs to ground.

Output loads recommended = 10 KΩ, Maximum Load = 5 KΩ.

Power Supply Turn-On/Turn-Off Sequence

Turn-on Sequence

Turn on negative supply first, then turn on the positive supply.

Turn-Off Sequence

Turn off positive supply first, then turn off the negative supply.

5

Handling Procedures

No special handling or precautions necessary above standard integrated circuits procedures.

Reliability

λ, Failure Rate ≤ .02%/1K hours at 75°C Tj

Thermal Resistance 0_{JC} = 47°C/Watt

5

DISPLAY MULTIPLEXER

DESCRIPTION

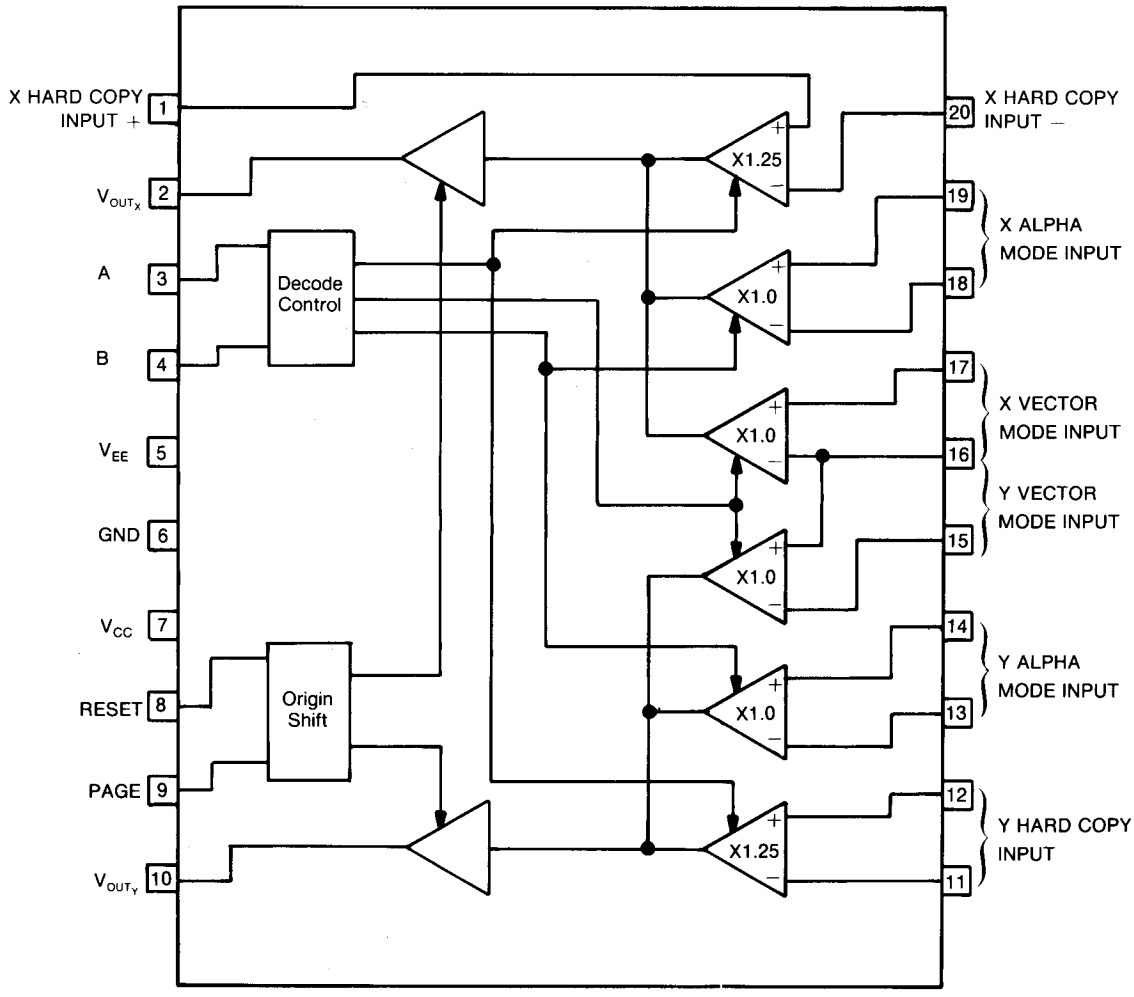
The 155-0154-00 transmits one of three sets of inputs (hardcopy, alphanumeric-mode, or vector mode) in accordance with the appropriate two-bit instruction on lines "A" and "B". Each input set has "X" and "Y" channels.

A counter sequences through eight offset positions each time a "page" (erase) signal is received. These offsets are added to the "X" and "Y" inputs to uniformly exercise the phosphor on all parts of the screen.

FEATURES

- Each channel has three differential voltage inputs and one single ended voltage output.
- Two logic inputs (A,B) are provided for differential voltage input.
- Provision for origin shifting the display for increased phosphor life is provided.

BLOCK DIAGRAM/PIN CONNECTIONS



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ABSOLUTE MAXIMUMS*

IDENTIFICATION	NOTES	VALUES	SYMBOLS
Offset Voltage	All channels	±90	mV
Bias Current	All channels	12	μA
Input Resistance	All channels (Minimum value)	0.88	MΩ
Common mode range		±1.0	V
Crosstalk	All channels	−60	dB
Voltage between V+ and V− terminals	Channel 1X, 1Y	±7.0	V
Voltage between V+ and V− terminals	Channel 2X, 2Y, 3X, 3Y	±7.0	V
Input risetime and falltime	All channels	10	μS
Digital input current	V_{in} = 0 volts, T_A = 75°C A, B, and Page Inputs	−1.6	mA
Digital input current	V_{in} = 5 volts, T_A = 75°C	40	μA

***T_A = 25°C unless otherwise noted.**

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ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
I_{CC}	Power Supply Current Note 1		+30	mA
I_{EE}	Power Supply Current Note 1	−25		mA
$V_{OUT(OS)}$	Output Offset Voltage Note 1	−90	+90	mV
A_V	Voltage Gain Channel 1X, 1Y Note 2		1.25 ±5%	
A_V	Voltage Gain Channel 2X, 2Y, 3X, 3Y Note 3		1.0 ±5%	
$G_{(LIN)}$	Gain Linearity Notes 2, 3, 4	−20	+20	mV
V_{SHIFT}	X Origin Shift Note 5	6.2	14.4	mV
V_{SHIFT}	Y Origin Shift Note 5	7.7	18.8	mV
$V_{SHIFT(MAX)}$	X Origin Shift (Max.) Note 5	57.6	86.4	mV
$V_{SHIFT(MAX)}$	Y Origin Shift (Max.) Note 5	72	108	mV

NOTE 1: $V_{CC} = +15$ V
$V_{EE} = -12$ V
$V_{IN} = 0$ V
$V_{RESET} = +5$ V
$T_A = +25°C$

NOTE 2: $V_{CC} = +15$ V
$V_{EE} = -12$ V
$V_{IN} = \pm 2.0$ V, ± 4.0 V
$V_{RESET} = +5$ V
V_A, V_B, See Truth Table
$T_A = +25°C$

$$A_V = \frac{V_{OUT} - V_{OUT(OS)}}{V_{IN}}$$

V_{IN} to one differential input. The other input is at ground. Input pair selected by V_A, V_B decode control.

NOTE 3: $V_{CC} = +15$ V
$V_{EE} = -12$ V
$V_{IN} = \pm 2.5$ V, ± 5.0 V
$V_{RESET} = +5$ V
V_A, V_B, See Truth Table
$T_A = +25°C$

$$A_V = \frac{V_{OUT} - V_{OUT(OS)}}{V_{IN}}$$

V_{IN} to one differential input. The other input is at ground. Input pair selected by V_A, V_B decode control.

TRUTH TABLE

V_A(3)	V_B(4)	$V_{IN(PIN\#S)}$	$V_{OUT(PIN\#S)}$
H	H	18, 19	2
H	H	14, 13	10
H	L	16, 17	2
H	L	16, 15	10
L	X	20, 1	2
L	X	12, 11	10

H = +5 V
L = 0 V

NOTE 4: Gain linearity is the difference in transfer function slope between 0% to 50% and 50% to 100% signal.

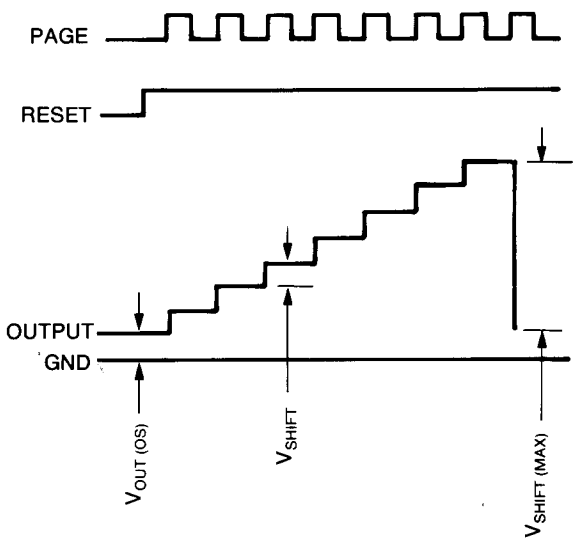
CH 1X, 1Y	CH 2X, 2Y, 3X, 3Y
$A_V = 1.25$ nominal	$A_V = 1.0$ nominal
$V_{IN(MAX)} = \pm 4.0$ V	$V_{IN(MAX)} = \pm 5.0$ V
$V_{IN(A)} = 0$ V	$V_{IN(A)} = 0$ V
$V_{IN(B)} = 2.0$ V	$V_{IN(B)} = 2.5$ V
$V_{IN(C)} = 4.0$ V	$V_{IN(C)} = 5.0$ V

$G_{(LIN)} = V_{OUT(C)} - 2\,V_{OUT(B)} - V_{OUT(A)}$

NOTE 5: $V_{CC} = +15$ V
$V_{EE} = -12$ V
$V_{IN} = 0$ V
V_{RESET} See Timing Diagram
V_{PAGE}
$t_A = +25°C$

TIMING DIAGRAM

Origin shift maximum ($V_{SHIFT(MAX)}$) is the output offset voltage, seven page pulses after the reset line goes high. V_{SHIFT} is with respect to the un-shifted output, as measured with the reset line held low. Origin shift (V_{SHIFT}) is the output voltage change caused by a single page pulse.



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APPLICATIONS INFORMATION

Input Protection

Amplifier sections 1X, 1Y, 2X, 2Y, 3X, and 3Y:

—Applied differential voltage at inputs; ≤7.0 volts.

Logic inputs A, B, Page, and Reset:

—Maximum Logic 0 current at V_{IN} = 0 Volts; $I_{IN} < -1.6$ mA
—Maximum Logic 1 current at V_{IN} 5 Volts; $I_{IN} < 40\ \mu A$

All inputs should have 5 KΩ series limiting during high temperature testing ($T_A > 75°C$).

Output Loading

Output Loading ≤ ±1 mA

Applied output potential ≤ ±5 Volts

Power Supply Turn-On/Turn-Off Sequence

Turn "on" sequence

First ..... −12/−15
Second ..... +15

Turn "off" sequence

First ..... +15
Second ..... −12/−15

Handling Procedures

All leads should be equipotential during handling to protect internal MOS cap structures.

Standard DIP mounting techniques should be employed.

Reliability Statement

λ, failure rate ≤.14%/1K hours at 75°CTj

θ_{jA} = 97.5°C/W

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5

TV SYNC GENERATOR

DESCRIPTION

This monolithic silicon (CMOS) device is a multi-standard broadcast television synchronous generator. It provides broadcast quality timing signals for TV test equipment.

FEATURES

- Programmed for timing standards
  - NTSC
  - PAL
  - PAL M
- Output signals include
  - synchronous signals required for TV broadcasting
  - timing for various test signals
  - synchronous counter chain from 64H to H
- CMOS silicon gate technology
- 40 Pin Ceramic DIP

ABSOLUTE MAXIMUMS

Voltage on any pin relative to V_{SS}	−0.3 to +12	V
Operating Temperature (Ambient)	0 to 75	°C
Storage Temperature	−65 to +150	°C
Power Dissipation	0.1	W
Operating Junction Temperature	0 to +80	°C

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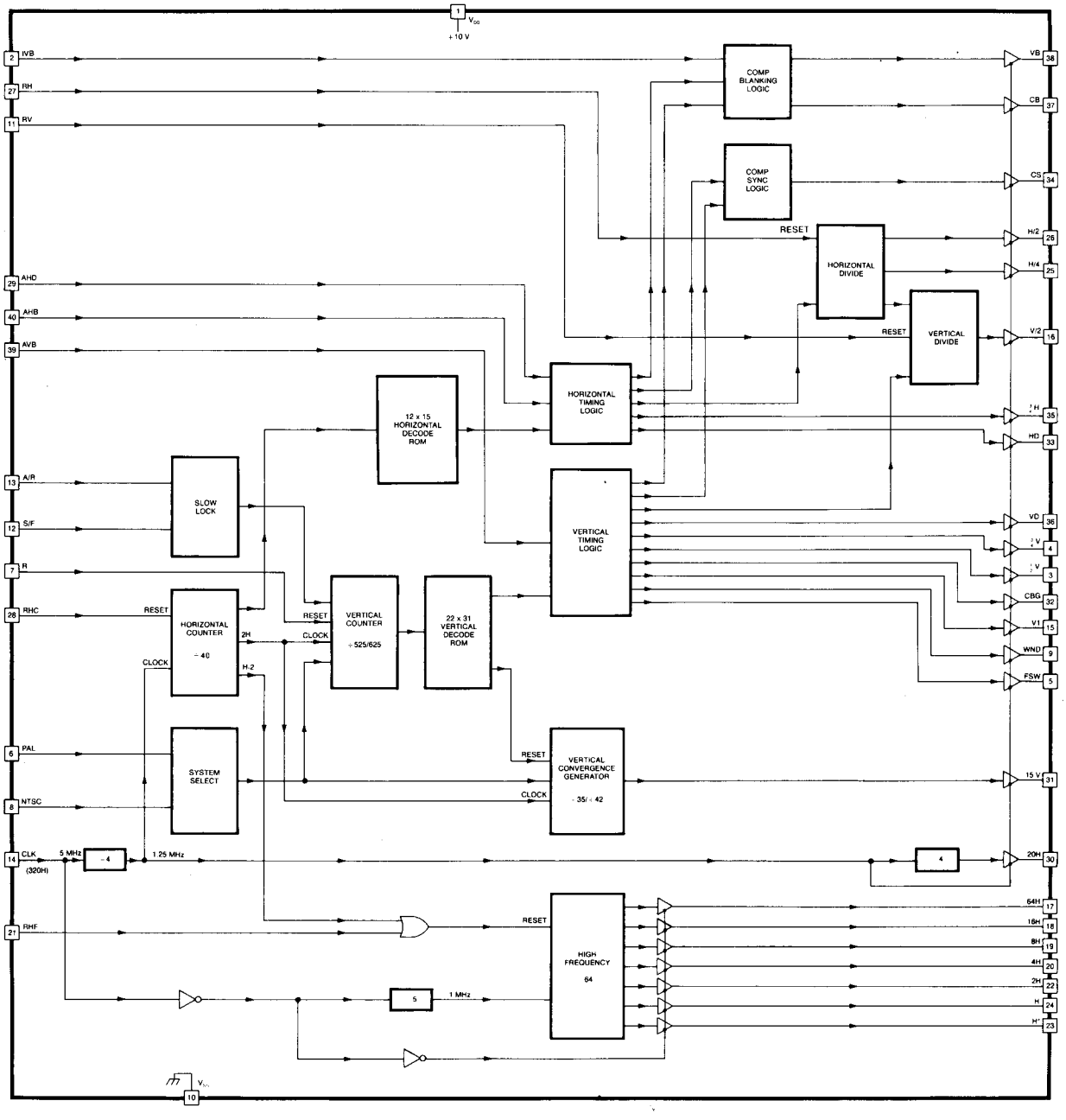
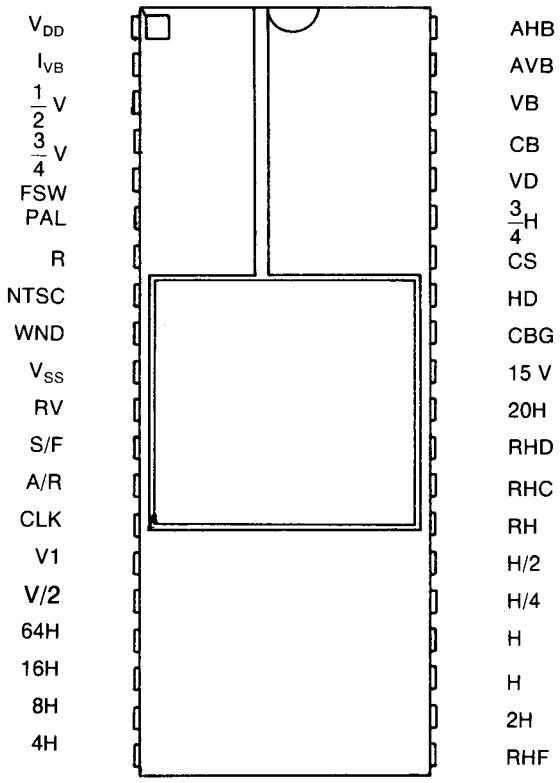
BLOCK DIAGRAM



TERMINAL IDENTIFICATION

PIN #	NAME	INPUT/OUTPUT	DESCRIPTION
1	V_{DD}		10 V Supply
2	I_{VB}	Input	Inhibit Vertical Blanking
3	1/2 V	Output	1/2 V Field Delay
4	3/4 V	Output	3/4 V Field Delay
5	FSW	Output	Field Square Wave
6	PAL	Input	PAL/PALM System Select
7	R	Input	Reset Vertical Counter
8	NTSC	Input	NTSC System Select
9	WND	Output	Window
10	V_{SS}		Ground
11	RV	Input	Reset V Divide
12	S/F	Input	Slow Lock
13	A/R	Input	Advance/Retard for Slow Lock
14	CLK	Input	5 MHz Clock
15	V1	Output	Field One Indicator
16	V/2	Output	
17	64H	Output	High Frequency Divider
18	16H	Output	High Frequency Divider
19	8H	Output	High Frequency Divider
20	4H	Output	High Frequency Divider
21	RHF	Input	High Frequency Reset/Disable
22	2H	Output	High Frequency Divider
23	H*	Output	High Frequency Divider
24	H	Output	High Frequency Divider
25	H/4	Output	
26	H/2	Output	
27	RH	Input	Reset H Divide
28	RHC	Input	Reset Horizontal Counter
29	AHD	Input	Advance Horizontal Drive
30	20H	Output	Horizontal Convergence
31	15 V	Output	Vertical Convergence
32	CBG	Output	Color Burst Gate
33	HD	Output	Horizontal Drive
34	CS	Output	Composite Sync
35	3/4H	Output	3/4 Line Delay
36	VD	Output	Vertical Drive
37	CB	Output	Composite Blanking
38	VB	Output	Vertical Blanking
39	AVB	Input	Advance Vertical Blanking
40	AHB	Input	Advance Horizontal Blanking

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
V_{IH}	Input High Voltage	.7 V_{DD}		V
V_{IL}	Input Low Voltage		.15 V_{DD}	V
I_{IL}	Input Low Current $V_{IN} = 0$*		±40	μA
I_{IH}	Input High Current (Except Clock) $V_{IN} = V_{DD}$*		±10	μA
$I_{IH\ (CLK)}$	Clock Input High Current $V_{IN} = V_{DD}$*		±10	μA
I_{OL}	Output Low Current $V_{OL} = .4$ V*		1.5	mA
I_{OH}	Output High Current $V_{OH} = V_{DD} - .5$ V*		1.5	mA
V_{SS}	Supply Voltage	Ground		
V_{DD}	Supply Voltage	9.5	10.5	V
I_{DD}	Static. All resets activated*		7	mA
I_{DD}	Dynamic—All resets disabled*		11	mA

NOTE: *V_{DD} = 10 V

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AC PARAMETERS

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
τ_R	Output Rise Time 10% → 90% V_{DD} = 10 V C_L = 50 pF		60*	nS
τ_F	Output Fall Time 10% → 90% V_{DD} = 10 V C_L = 50 pF		60*	nS
τ_Δ(HF)	Differential Delay Between Outputs $C_{L1} = C_{L2}$		100†	nS
τ_Δ	Differential Delay Between 64H and any of the 16H, 8H, 4H, 2H, H*, and H Outputs		±10†	nS
$\Delta_{\tau\Delta}$	Change in τ_Δ with Time and Temperature 0°C ≤ Temp ≥ 75°C		10†	nS
τ_{CS}	Composite Sync Pulse Width 50% Point f_{CLK} = 5.034 MHz	4.65	4.72**	nS
f_{CLK}	Clock Input Frequency		5.034 (Nom)	MHz
τ_{CLK}	τ_R and τ_F at Clock Input 10% → 90%		20	nS
τ_D	Delay from Clock to Output 50% Point		120	nS

NOTES: ***Value guaranteed by calculating from DC current measurement**

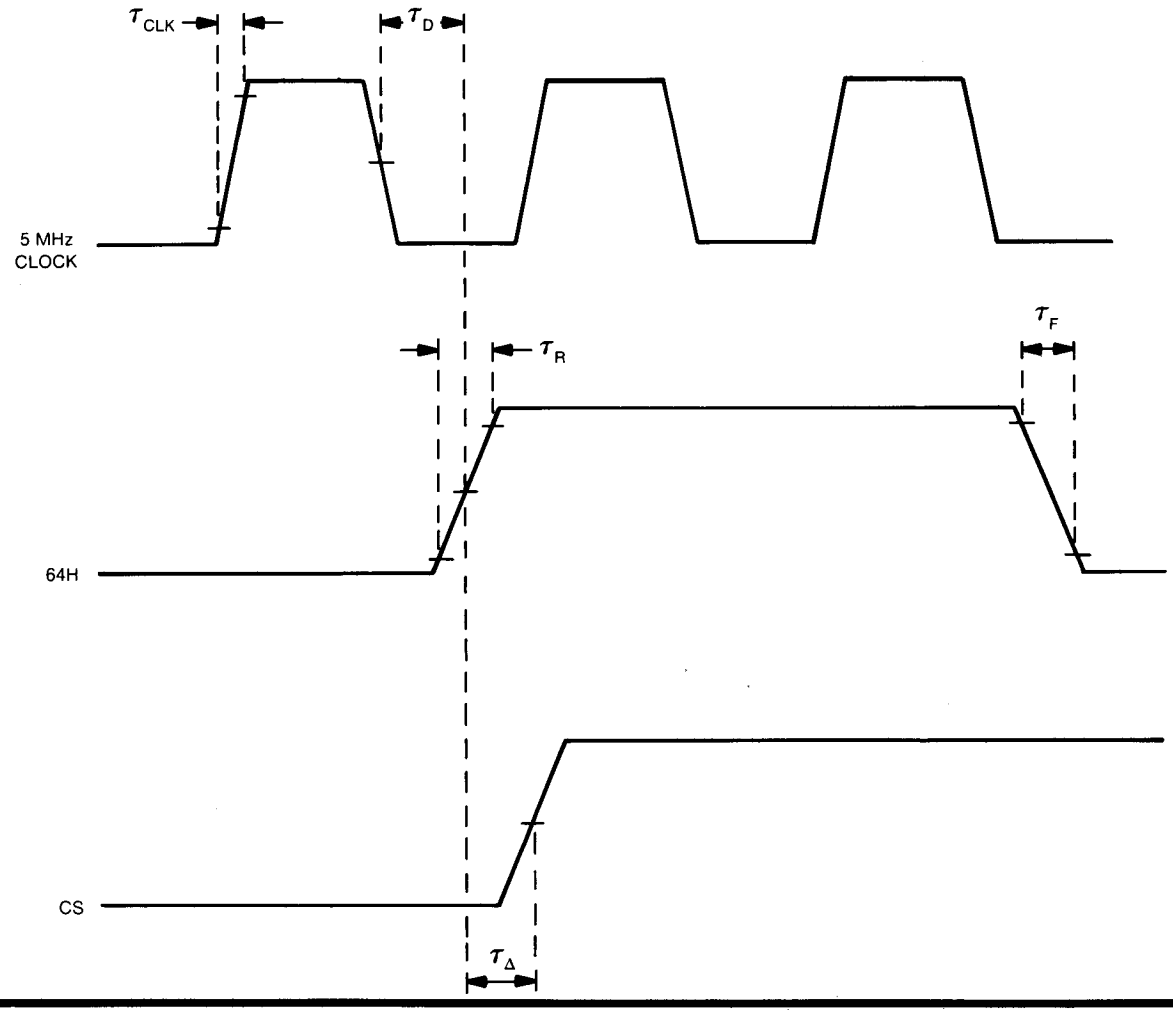
†Measurement on typical part; worst case calculated to be less than maximum value

****Values assume clock is a perfect square wave**

DC PARAMETERS

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
V_{IH}	Input High Voltage	.7 V_{DD}		
V_{IL}	Input Low Voltage		.15 V_{DD}	
I_{IL}	Input Low Current $V_{IN} = 0$*		±10	μA
I_{IH}	Input High Current (Except Clock) $V_{IN} = V_{DD}$*		40	μA
$I_{IH\ (CLK)}$	Clock Input High Current* $V_{IN} = V_{DD}$		±10	μA
I_{OL}	Output Low Current V_{OL} = .4 V*		1.5	mA
I_{OH}	Output High Current* $V_{OH} = V_{DD} - .5$ V		1.5	mA

*V_{DD} = 10 V



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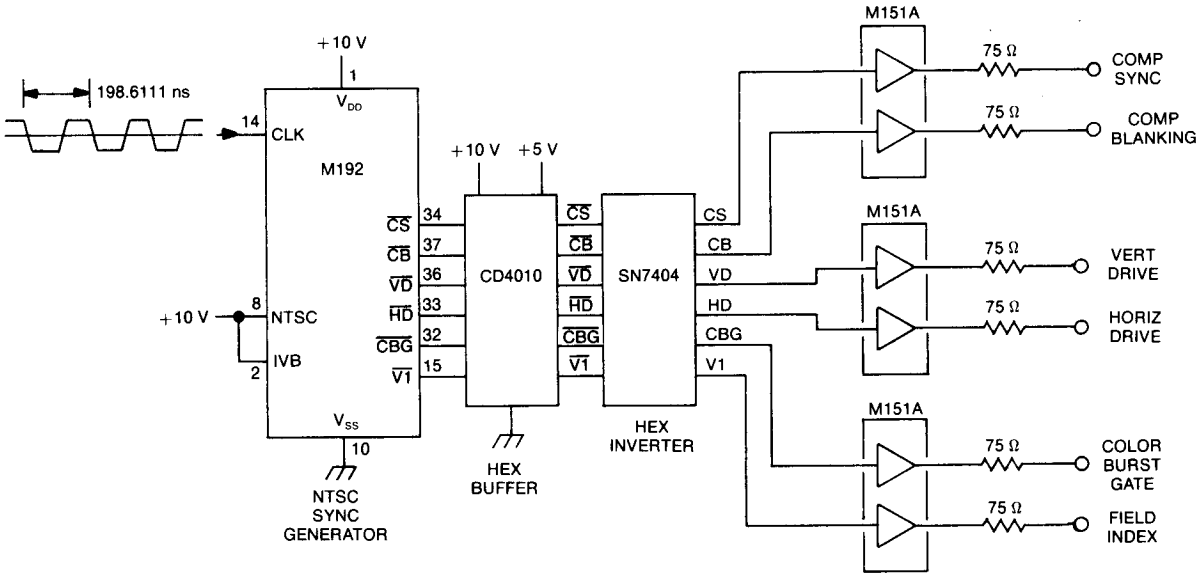
APPLICATIONS INFORMATION



RELIABILITY

λ, .061%/1K hours at 75°C Tj

θ_{DC} = 25°C/Watt

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TRIGGER CIRCUIT

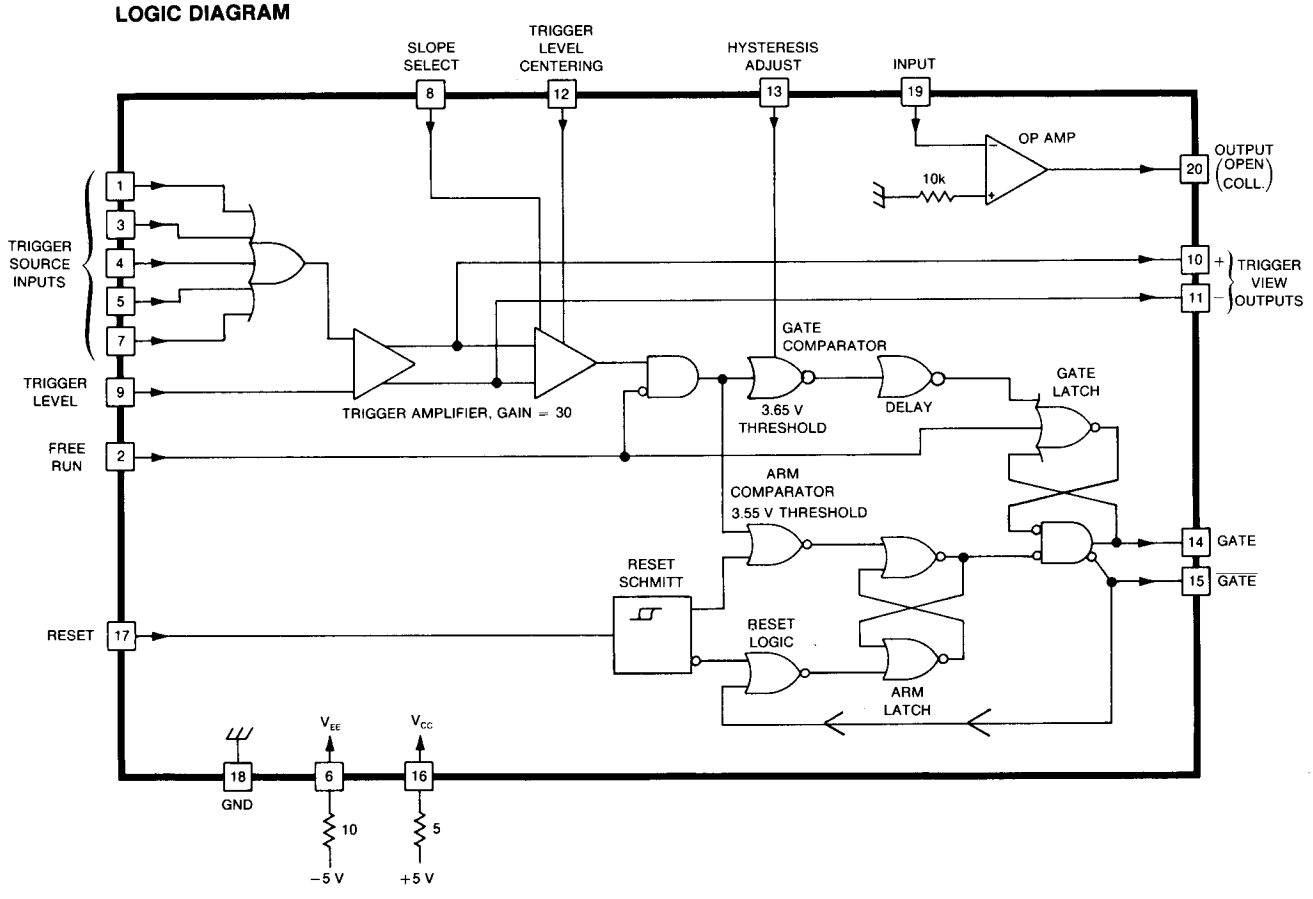
DESCRIPTION

This integrated circuit is a trigger for oscilloscopes ⩾100 MHz bandwidth. It includes an operational amplifier with open-loop gain of 500.

FEATURES

- Slope selection
- Gate output and $\overline{\text{gate output}}$ are ECL levels
- Hysteresis adjustment
- Trigger level centering
- Free run input
- Trigger view outputs
- 5 mV sensitivity
- Five inputs
- 310 mW power dissipation

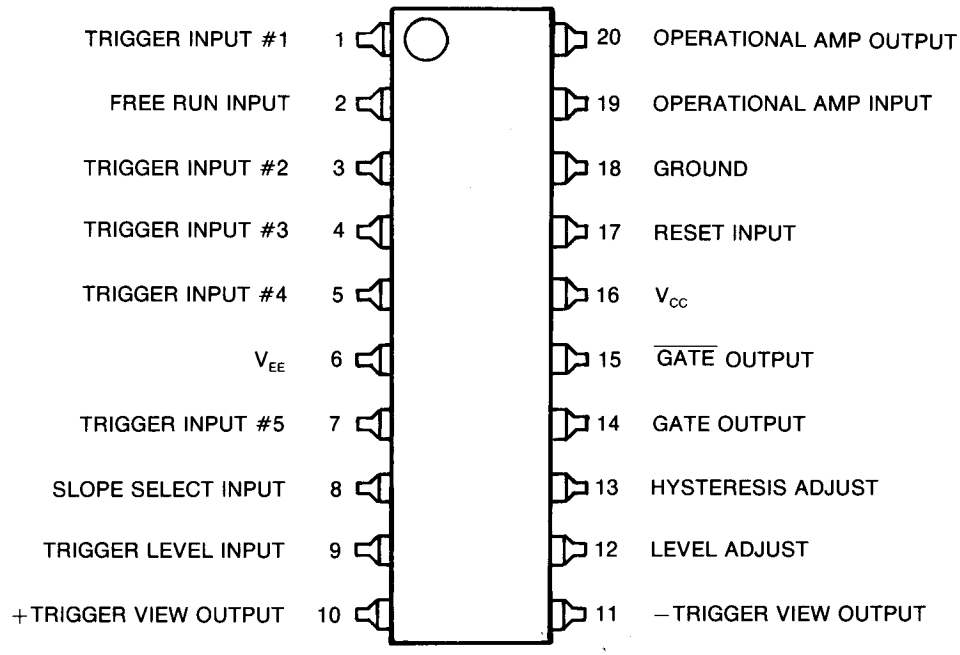
LOGIC DIAGRAM



ABSOLUTE MAXIMUMS

Storage Temperature (T_{SG})	−55°C to +125°C
Operating Ambient Temperature (T_A)	−15°C to +85°C
Maximum Power Dissipation (P_D)	462 mW
Derating Factor (Above 70°C Ambient)	10.3 mW/°C
V_{CC} (Pin #16)	+5.25 V
V_{EE} (Pin #6)	−5.25 V
Trigger Input Voltage	+0.7 V
(Pins #1, #3 #4, #5, and #7)	−2.0 V
Trigger Level Input Voltage (Pin #9)	+0.7 V
	−2.0 V
Free-Run Input Voltage (Pin #2)	0 to V_{CC}
Slope Select Input Voltage (Pin #8)	±5.5 V
Reset Input Voltage (Pin #17)	0 V to V_{CC}

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS

PIN #	PARAMETER	MIN	MAX	UNITS
16	V_{CC} Power Supply Current	41.5	77	mA
6	V_{EE} Power Supply Current	8.5	15.5	mA
——	Logic Test	Refer to (Truth Table)		
14	Gate Output High Voltage (V_{OH})	3.7	4.2	V
14	Gate Output Low Voltage (V_{OL})	2.75	3.25	V
15	$\overline{\text{Gate}}$ Output High Voltage (V_{OH})	3.7	4.2	V
15	$\overline{\text{Gate}}$ Output Low Voltage (V_{OL})	2.75	3.25	V
1, 3, 4, 5, 7	Trigger Input Bias Current	0	30	μA
10, 11	Trigger View Output Offsets	−50	+50	mV
10, 11	Trigger View Output Gain, +Slope	4	6.5	——
10, 11	Trigger View Output Gain, −Slope	4	6.5	——
10, 11	Trigger View Output Swing	.5	1.5	V
1, 3, 4, 5, 7	Trigger Input Leakage Currents	0	10	μA
9	Trigger Level Input Bias Current	0	50	μA
2	Free Run Input Current	.5	1.5	mA
8	Slope Select Input Current	.2	.6	mA
17	Reset Input Current	0	1.0	mA
19, 20	Operational Amplifier Gain	9.5	10.5	——
19	Operational Amplifier Input Offset	−40	+40	mV
19	Operational Amplifier Input Bias Current	0	10	μA
20	Operational Amplifier Output Swing	1.0	——	V
1, 9	+Trigger Slope Absolute Offset	−60	60	mV
1, 9	+Slope Hysteresis	0	10	mV
1, 9	−Trigger Slope Absolute Offset	−60	60	mV
1, 9	−Slope Hysteresis	0	10	mV
1, 9	+Slope to −Slope Offset	−25	25	mV

APPLICATIONS INFORMATION

PRODUCT PRECAUTIONS

Input Protection

-3 V $\leq$Trigger Inputs (For Trigger Level Input at Ground)
$V_{EE} \leq$Slope Select Input $\leq V_{CC}$
-3 V $\leq$Free Run Input $\leq V_{CC}$
0 V $\leq$Reset Input $\leq V_{CC}$
-3.7 V $\leq$OP Amplifier Input $\leq +3.7$ V

Output Loading

DO NOT short Trigger View Outputs to V_{EE}.
Trigger View Output $\leq +3$ V.
DO NOT short gate output and $\overline{\text{gate}}$ output to ground or V_{EE}.
DO NOT allow DC output loading on Trigger View outputs, gate output, and $\overline{\text{gate}}$ output to exceed 6 mA.
DO NOT short OP Amplifier output to V_{CC}.

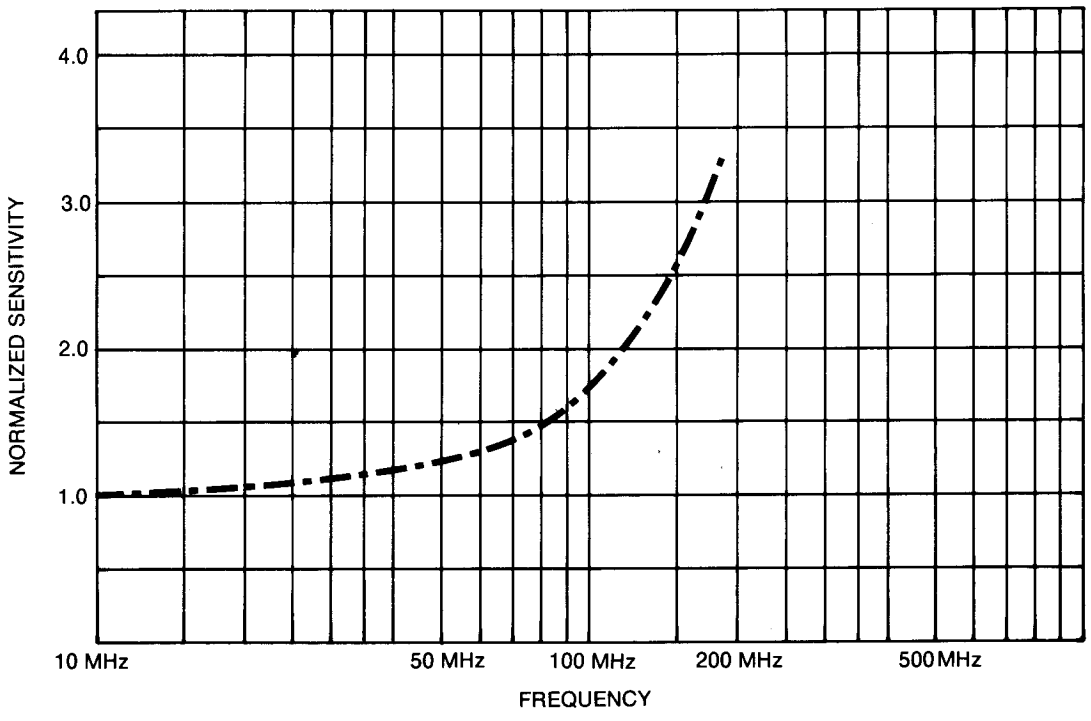
Power Supply Turn-On/Turn-Off Sequence

Two power supplies; NO power supply turn-on/turn-off sequence sensitive.

Handling Procedures

No special static precautions are necessary.

NORMALIZED SENSITIVITY vs FREQUENCY

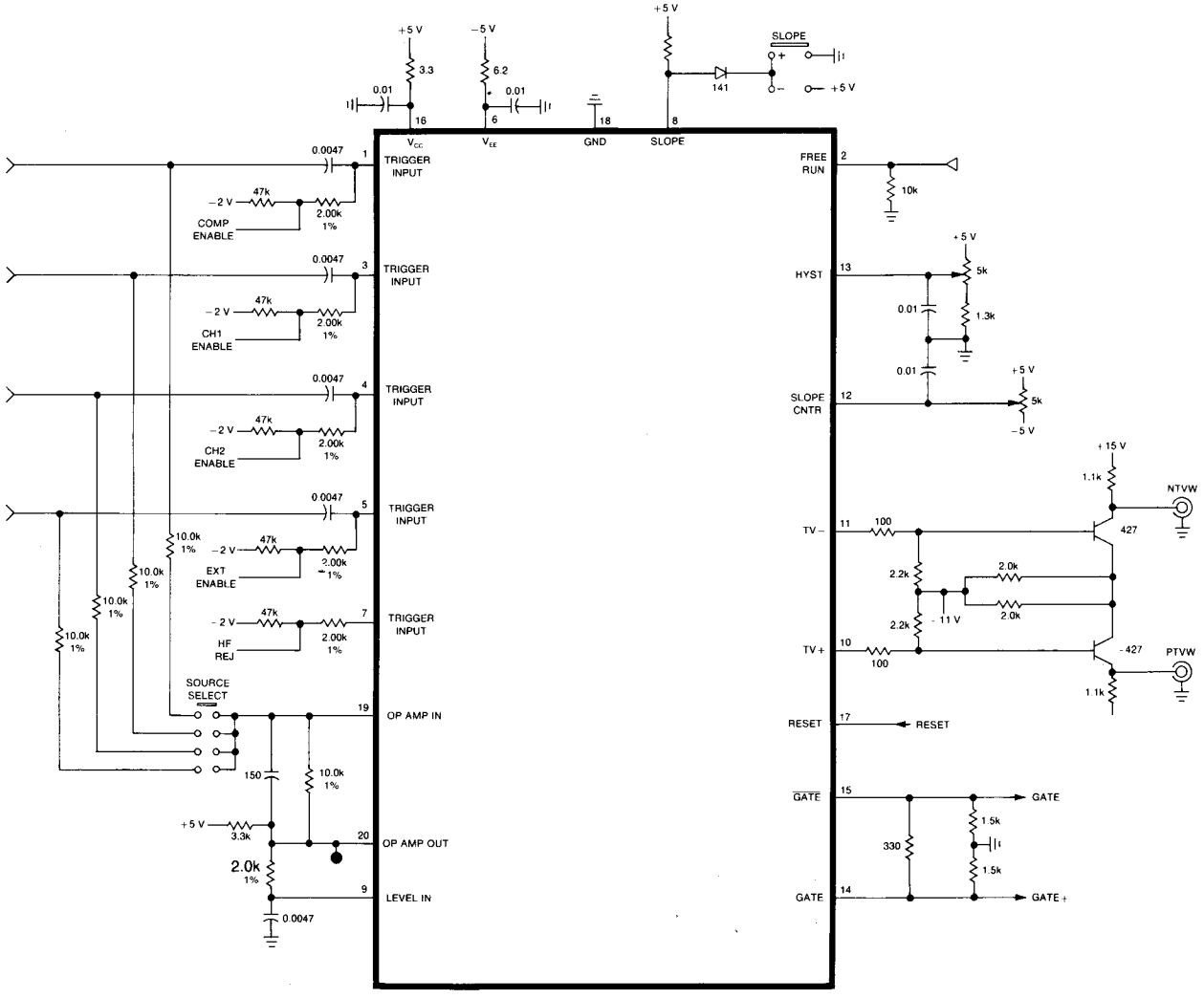


	SLOPE	RESET	FREE RUN	INPUT #1	INPUT #2	INPUT #3	INPUT #4	INPUT #5	GATE OUT	GATE OUT	FUNCTION	
1.000	0	1	0	0	0	0	0	0	0	1	. . .	RESET	
2.000	0	0	0	0	0	0	0	0	0	1	. . .	ARM	
3.000	0	0	0	1	0	0	0	0	1	0	. . .	+TRIGGER	
4.000	0	0	0	0	0	0	0	0	1	0	. . .	LATCH	CHECKS INPUT #1
5.000	1	1	0	0	0	0	0	0	0	1	. . .	RESET	
6.000	1	0	0	1	0	0	0	0	0	1	. . .	ARM	
7.000	1	0	0	0	0	0	0	0	1	0	. . .	−TRIGGER	
8.000	1	0	0	1	0	0	0	0	1	0	. . .	LATCH	
9.000	0	1	0	0	0	0	0	0	0	1	. . .	RESET	
10.000	0	0	0	0	0	0	0	0	0	1	. . .	ARM	
11.000	0	0	0	0	1	0	0	0	1	0	. . .	+TRIGGER	
12.000	0	0	0	0	0	0	0	0	1	0	. . .	LATCH	CHECKS INPUT #2
13.000	1	1	0	0	0	0	0	0	0	1	. . .	RESET	
14.000	1	0	0	0	1	0	0	0	0	1	. . .	ARM	
15.000	1	0	0	0	0	0	0	0	1	0	. . .	−TRIGGER	
16.000	1	0	0	0	1	0	0	0	1	0	. . .	LATCH	
17.000	0	1	0	0	0	0	0	0	0	1	. . .	RESET	
18.000	0	0	0	0	0	0	0	0	0	1	. . .	ARM	
19.000	0	0	0	0	0	1	0	0	1	0	. . .	+TRIGGER	
20.000	0	0	0	0	0	0	0	0	1	0	. . .	LATCH	CHECKS INPUT #3
21.000	1	1	0	0	0	0	0	0	0	1	. . .	RESET	
22.000	1	0	0	0	0	1	0	0	0	1	. . .	ARM	
23.000	1	0	0	0	0	0	0	0	1	0	. . .	−TRIGGER	
24.000	1	0	0	0	0	1	0	0	1	0	. . .	LATCH	
25.000	0	1	0	0	0	0	0	0	0	1	. . .	RESET	
26.000	0	0	0	0	0	0	0	0	0	1	. . .	ARM	
27.000	0	0	0	0	0	0	1	0	1	0	. . .	+TRIGGER	
28.000	0	0	0	0	0	0	0	0	1	0	. . .	LATCH	CHECKS INPUT #4
29.000	1	1	0	0	0	0	0	0	0	1	. . .	RESET	
30.000	1	0	0	0	0	0	1	0	0	1	. . .	ARM	
31.000	1	0	0	0	0	0	0	0	1	0	. . .	−TRIGGER	
32.000	1	0	0	0	0	0	1	0	1	0	. . .	LATCH	
33.000	0	1	0	0	0	0	0	0	0	1	. . .	RESET	
34.000	0	0	0	0	0	0	0	0	0	1	. . .	ARM	
35.000	0	0	0	0	0	0	0	1	1	0	. . .	+TRIGGER	
36.000	0	0	0	0	0	0	0	0	1	0	. . .	LATCH	CHECKS INPUT #5
37.000	1	1	0	0	0	0	0	0	0	1	. . .	RESET	
38.000	1	0	0	0	0	0	0	1	0	1	. . .	ARM	
39.000	1	0	0	0	0	0	0	0	1	0	. . .	−TRIGGER	
40.000	1	0	0	0	0	0	0	1	1	0	. . .	LATCH	
41.000	0	0	1	1	0	0	0	0	1	0	. . .	FREE RUN +SLOPE	
42.000	0	1	1	1	0	0	0	0	0	1	. . .	RESET OVER-RIDE	
43.000	1	0	1	1	0	0	0	0	1	0	. . .	FREE RUN −SLOPE	
44.000	1	1	1	1	0	0	0	0	0	1	. . .	RESET OVER-RIDE	

Logic Levels for Truth Table

PIN NAME	LOGICAL "0"	LOGICAL "1"
Slope Select Input	−1.0 V	+1.0 V
Reset Input	3.25 V	4.0 V
Free Run Input	500 mV	——
Inputs #1—#5	−2.0 V	+50 mV
Gate Output	2.75 V—3.25 V	3.7 V—4.2 V
$\overline{\text{Gate}}$ Output	2.75 V—3.25 V	3.7 V—4.2 V

TYPICAL APPLICATION



RELIABILITY

λ failure rate ≤.02%/1K hours at 75°C T_j
Thermal resistance, θ_{DA} 97 °C/W

LOGIC ANALYZER INPUT CIRCUIT

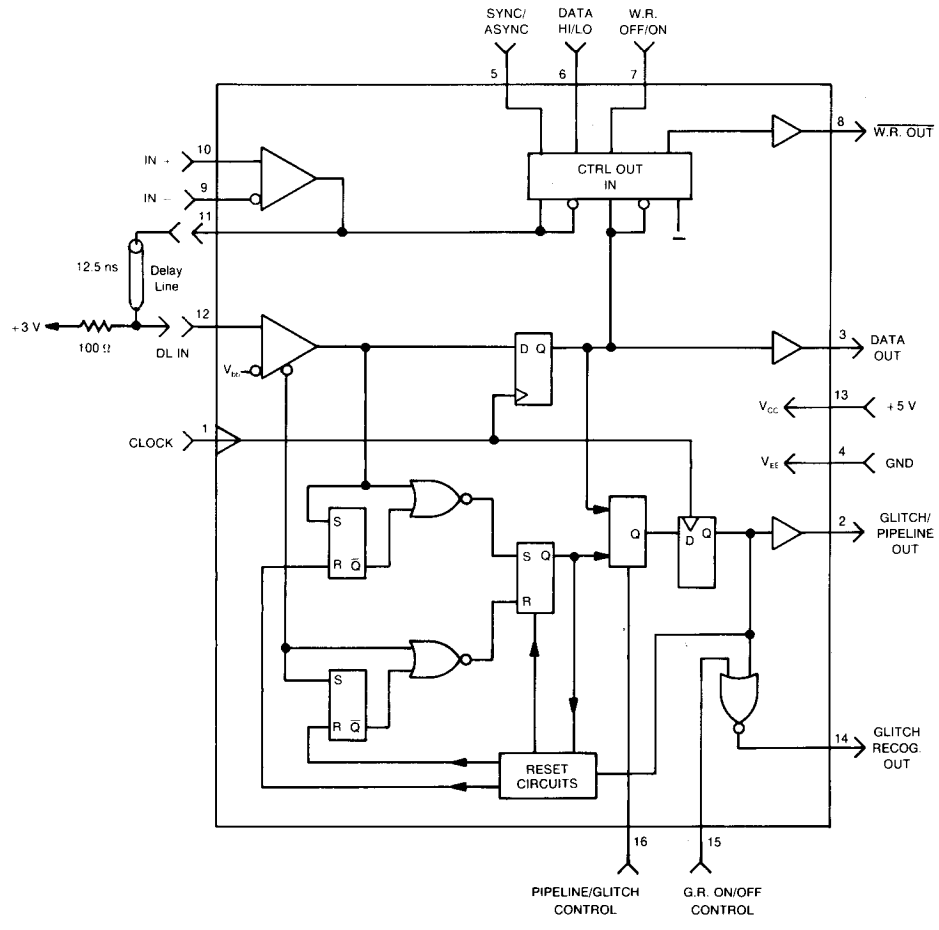
DESCRIPTION

The 155-0215-00 is a Logic Analyzer Input circuit with glitch latch capability. The circuit is packaged in a 16-pin DIP.

FEATURES

- Differential input and delay line port.
- Data latch and output.
- Word recognizer with control of syn/asyc and Hi/Off/Lo.
- Second order glitch detection with on/off control.
- A pipeline mode which uses the glitch memory for data, with an extra stage of latch, in lieu of the glitch detector. This matches instrument characteristics for synchronous data acquisition.

BLOCK DIAGRAM



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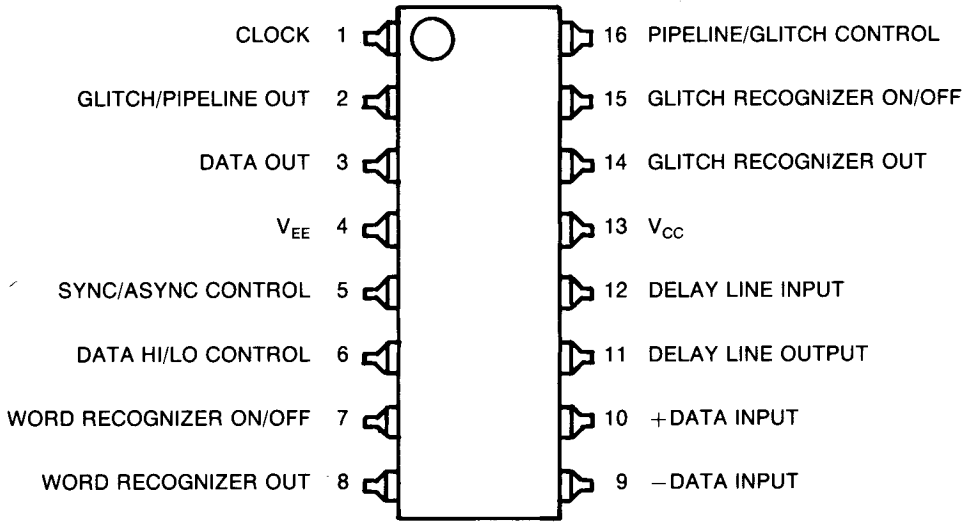
ABSOLUTE MAXIMUM

SYMBOL	IDENTIFICATION	NOTES	VALUES	UNITS
T_{SG}	Storage Temperature		−55 to 125	°C
T_A	Operating Temperature		−15 to 80	°C
P_D	Power Dissipation	at 80°C Ambient	470	mW
$V_{CC}-V_{EE}$	Supply Voltage	Maximum Pos Voltage	+5.5	V
V_I	Input Voltage	All input pins	V_{EE} to V_{CC}	
I_O	Output Current	$V_{CC}-V_{EE}$=5.0 V any output	15.0	mA
T_J		Maximum	125	°C

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS*

PIN #	PARAMETER	MIN	MAX	UNITS
13	Power Supply Current (Note 1) V_{EE} V_{LOAD}	20 0	70 25	mA mA
11	Delay Line Output Logical Low Level (Note 3)	3.0	3.4	V
3	Data Output Logical Low Level (Note 3)	3.0	3.4	V
2	Glitch/Pipeline Output Logical Low Level (Note 3)	3.0	3.4	V
14	Glitch Recognizer Logical Low Level (Note 3)	3.0	3.4	V
8	Word Recognizer Output Logical Low Level (Note 3)	3.0	3.4	V
11	Delay Output Logical High Level (Note 2)	4.0	4.3	V
3	Data Output Logical High Level (Note 2)	4.0	4.3	V
2	Glitch/Pipeline Output Logical High Level (Note 2)	4.0	4.3	V
14	Glitch Recognizer Output Logical High Level (Note 2)	4.0	4.3	V
8	Word Recognizer Output Logical High Level (Note 2)	4.0	4.3	V
10	Data Input Bias Current (Note 4) V_{IN} = 3.895 V	3	25	μA
9	Negative Input Bias Current (Note 4) V_{IN} = 3.895 V	3	25	μA
12	Delay Line Input Bias Current (Note 4) V_{IN} = 3.895 V	3	25	μA
1	Clock Input Bias Current (Note 4) V_{IN} = 3.895 V	3	25	μA
7	Word Recognizer Off/On Input Bias Current (Note 4) V_{IN} = 4.00 V	3	500	μA
6	Data High/Low Input Bias Current (Note 4) V_{IN} = 4.00 V	3	500	μA
15	Glitch Recognizer Off/On Input Bias Current (Note 4) V_{IN} = 4.00 V	3	500	μA
5	Sync/Async Select Input Bias Current (Note 4) V_{IN} = 2.40 V	3	410	μA
16	Pipeline/Glitch Select Input Bias Current (Note 4) V_{IN} = 2.40 V	——	410	μA
1,3	Clock to Data Out	2.5	5.5	nS
1,2	Clock to Glitch/Pipeline Out (Mode = Glitch)	2.5	5.5	nS
1,2	Clock to Pipeline Out (Mode = Pipeline)	2.5	5.5	nS
2	Minimum Recognizable Glitch Width, first order measured or second order measured from first to second transition, at 50% amplitude points—differential inputs swinging from V_{CC} = 0.9 ± 0.1 V to V_{CC} = 1.6 V ± 0.1 V	4	——	nS
2	Minimum Recognizable Glitch Width, second order measured from second to third transition, at 50% amplitude points—differential inputs swinging from V_{CC} = 0.9 V ± 0.1 V to V_{CC} = 1.6 V ± 0.1 V	5	——	nS

Unless otherwise noted, V_{CC} = +5 V ±10 mV, T_A = 25°C, V_{EE} = 0 V.

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NOTE 1

All outputs in logical low state, load conditions = 100 Ω to +3 V. V_{CC} = 5.0 Volts. T_A = 25°C.

NOTE 2

R_1 = 100 Ω to +3.0 volts. Desired output set to high state. Measure voltage on pin specified. V_{CC} must be accurate to ± 10 mV.

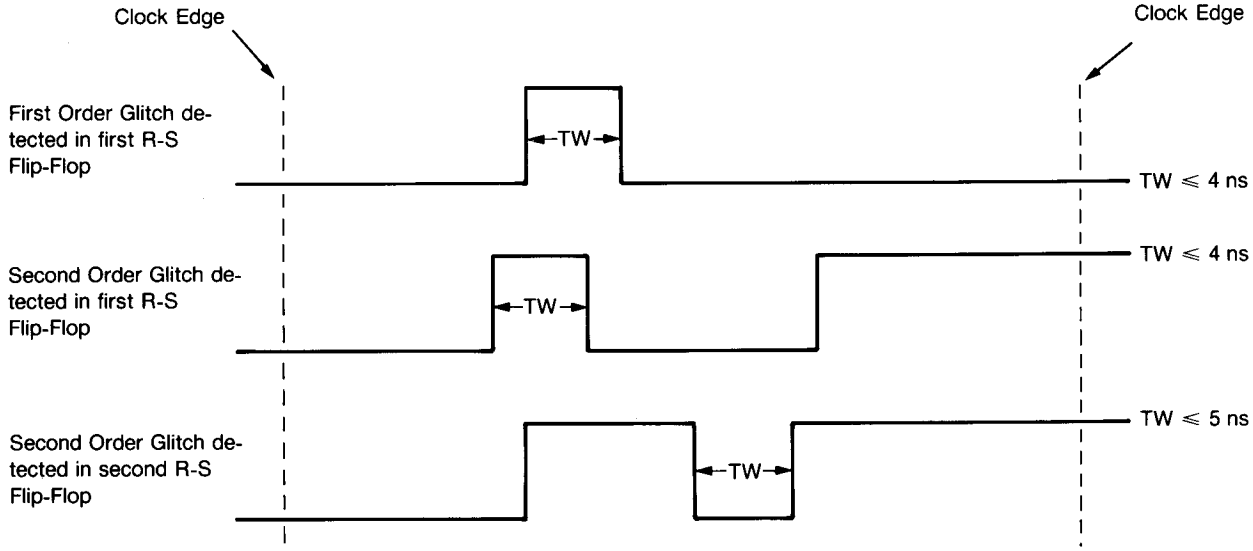
NOTE 3

R_1 = 100 Ω to 3 volts. All outputs in low state. Measure voltage on pin specified. V_{CC} must be accurate to ± 10 mV.

NOTE 4

Same input conditions as Note #1. Measure current on pin specified.

In order to detect a glitch, the first and second R-S Flip Flops both have to be set. Therefore, two tests are necessary to detect the minimum set time in (either of) the first R-S Flip Flops or the second R-S Flip-Flop.



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APPLICATIONS INFORMATION

SYMBOL	FUNCTION	MEASURED TYPICAL	CALCULATED WORST CASE
T_{CD}	Clock to Data Out	4.5 nS	7.6 nS
T_{DAWR}	Data to Async Word Recognizer Out	3.5 nS	6.1 nS
T_{CSR}	Clock to Synchronous Recognizer Out	5.4 nS	8.5 nS
T_{CG}	Clock to Glitch Pipeline Out	4.4 nS	9.0 nS
T_{CGR}	Clock to Glitch Recognizer Out	4.3 nS	9.8 nS
T_{PIPE}	Clock to Pipeline Out	4.6 nS	8.6 nS
T_{DS}	Data Set-up Time Delay line input to clock input	0.5 nS	0.5 nS
T_{DH}	Data Hold Time Clock input to delay line input	0.0 nS	0.0 nS
T_{DDL}	Data In to Delay Line Driver Out	1.9 nS	2.7 nS

APPLICATIONS INFORMATION (cont)

Application Symbol Definition

T_{CD}, T_{DAWR}, T_{CSR}, T_{CG}, T_{CGR}, T_{PIPE}, and T_{DDL}: Time delays from data or clock input to stated output change.

T_{DS}: Data set-up time. Time before clock edge for which stationary input data will produce matching data output after the clock edge.

T_{DH}: Time after clock edge for which data must be held stationary in order not to affect the data output after clock edge.

Calculated Worst Case Assumptions

Spice computer modeled

$T_j = 110°C$

Beta Max = 200 (For maximum F_T and maximum base resistance)

Resistor Tolerance = +30%

Maximum Junction Capacitance

PRODUCT PRECAUTIONS

Input Protection

DO NOT exceed V_{CC} supply on any input at any time.

Output Loading

DO NOT short outputs to V_{EE}.

DO NOT allow output capacitance to exceed 200 pF.

Power Supply Turn On/Turn Off Sequence

Single Supply—DO NOT exceed absolute maximum rating.

RELIABILITY

λ, Failure Rate $\leq$ .0413%/1K Hrs. at 75°C T_j

Thermal resistance junction to case.
$\theta_{jc} = 94°C/W$

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INPUT AMPLIFIER

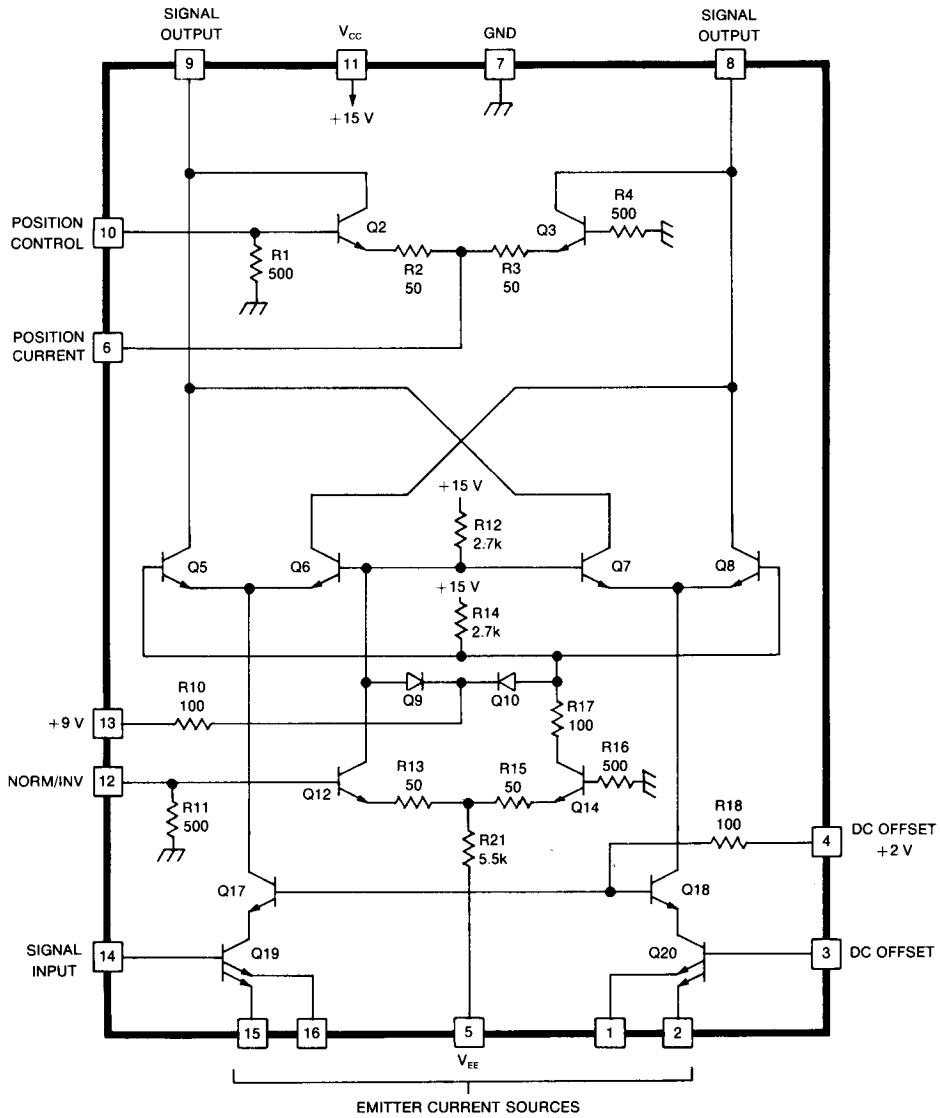
DESCRIPTION

The 155-0217-00 is a transconductance amplifier with gain control, and provision is made for offset and positioning control.

FEATURES

- Variable gain control
- Offset and positioning control inputs
- 16 pin dual-in-line package

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUMS

Environmental

SYMBOL	IDENTIFICATION	VALUES	UNITS
T_{stg}	Storage Temperature	−55 to +125	°C
T_a	Operating Ambient Temperature Range	0 to 70	°C

Electrical

BV_{EBO}	Emitter-Base Breakdown Voltage	5.8	V
V_{CE}	Collector-Emitter Voltage	15	V
BV_{CS}	Positive Voltage on pins 8, 9, and 11 W.R.T. Pin 5	30	V
	Pin 13 Voltage W.R.T. Pin 7	10	V
	Voltage on Pins 10 and 12 W.R.T. Pin 7	5	V
I_{total}	Total Current from Pin 8 or Pin 9	20	mA
P_D	Total Device Power Dissipation	300	mW

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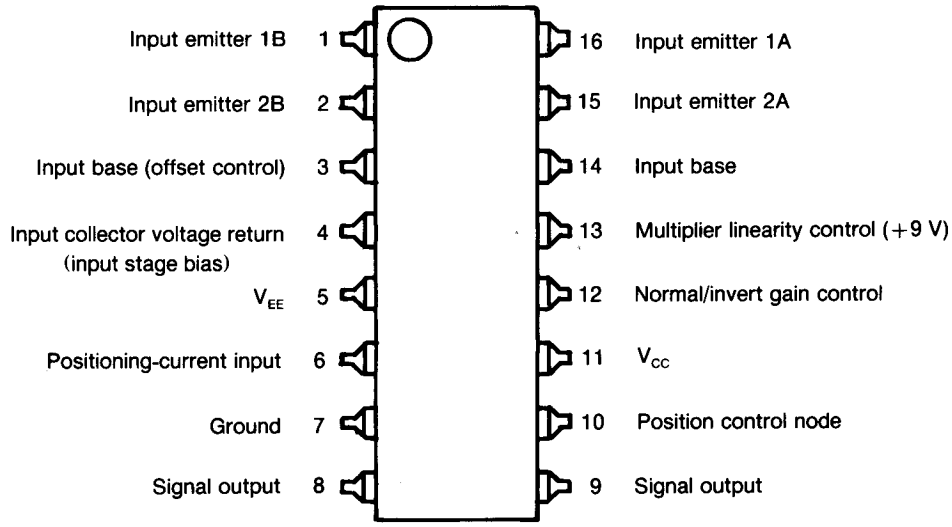
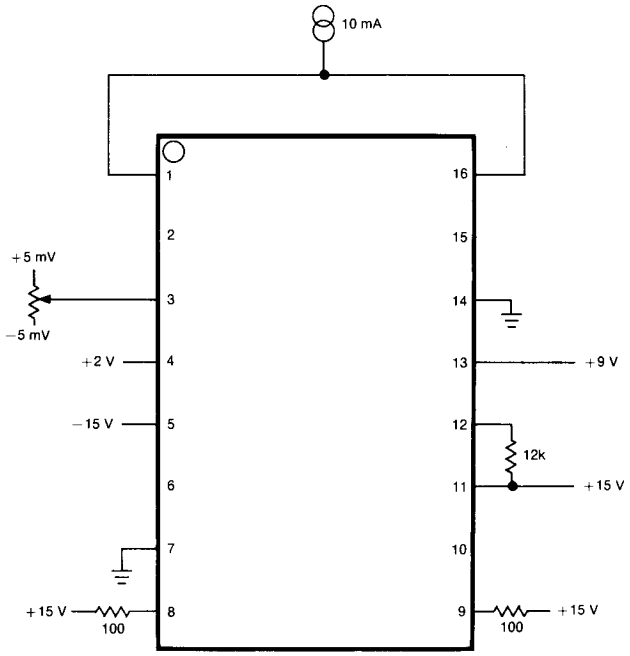
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

Parameter Symbol	Parameter Name and Conditions of Measurement	Min Value	Max Value	Unit of Meas.	Pin Meas.
R_E	Emitter Bulk Resistance (typ. 3.5 Ω)			Ω	1, 2, 15, 16
V_{IOS}	Input Offset Voltage (see note 1)		±5.0	mV	3
I_{IOS}	Input Offset Current (see note 1)		50	μA	3, 14
h_{fb}	Common-Base Forward Current Gain	0.95			8 & 9 Gnd. 1, 16 or 2, 15
t_r	Risetime (typical 800 ps)			ps	
$I_{O.D.}$	Output Current Differential (Null Supp.)		±33.0	μA	8, 9
$I_{G.C.NORM}$	Gain Control Current (Max. Norm.)	200	350	μA	12
$I_{G.C.INV.}$	Gain Control Current (Max. Inv.)	−350	−200	μA	12
$I_{Z.G.}$	Gain Control Current (Zero Gain)		±48	μA	12
$V_{A.C.}$	Position Control Voltage		±50	mV	10

NOTE 1:



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Input Offset Voltage

Set differential output voltage (Pins 8 & 9) to zero, measure Pin 3 voltage.

Input Offset Current

Insert current measuring devices in leads of Pins 3 & 14. Set differential output voltage to zero, measure ABSOLUTE current difference between Pin 3 and Pin 14.

Output Current Differential

Apply input offset voltage to Pin 3. Then measure output current differential at any gain setting (Pin 12).

Position Control Voltage

Source Pin 6 with 2 mA. Set voltage at Pin 10 such that differential output current is zero. Measure voltage at Pin 10.

Reliability

λ Failure rate $\leq$.02%/1K hours at 75°C T_j
θ_{jc} junction to case, 50°C/W

VERTICAL OUTPUT DRIVER

DESCRIPTION

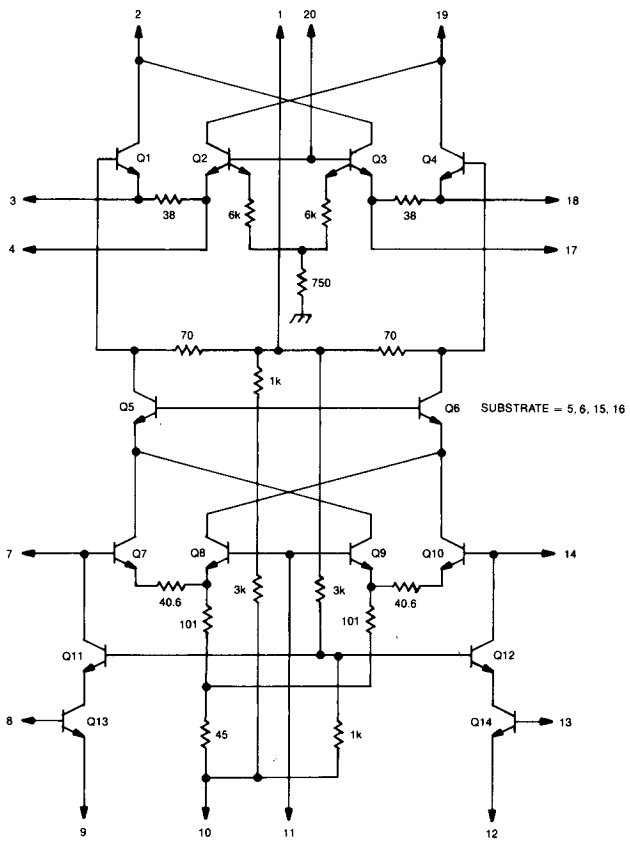
The 155-0218-00 is a vertical output driver for use in up to 150 mHz instruments. As such it provides all current gain for the vertical output system. Common-base output followers and load resistors (re. 155-0219-00) interface the part to a Crt.

The 155-0218-00 is virtually identical to the die used in the 155-0077-00 and 155-0115-00. The only difference being a doubling of second and third stage nichrome emitter values in the 155-0218-00. This change increases linearity at the lower bias currents appropriate for 50—150 MHz application.

FEATURES

- Cost effective vertical output
- 80mA output current
- Low power
- 1 nS Risetime

Schematic (Figure 1)



PACKAGE PINOUT FOR 20 PIN DIP

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ABSOLUTE MAXIMUMS

Unless stated otherwise, ambient temperature = 25°C.

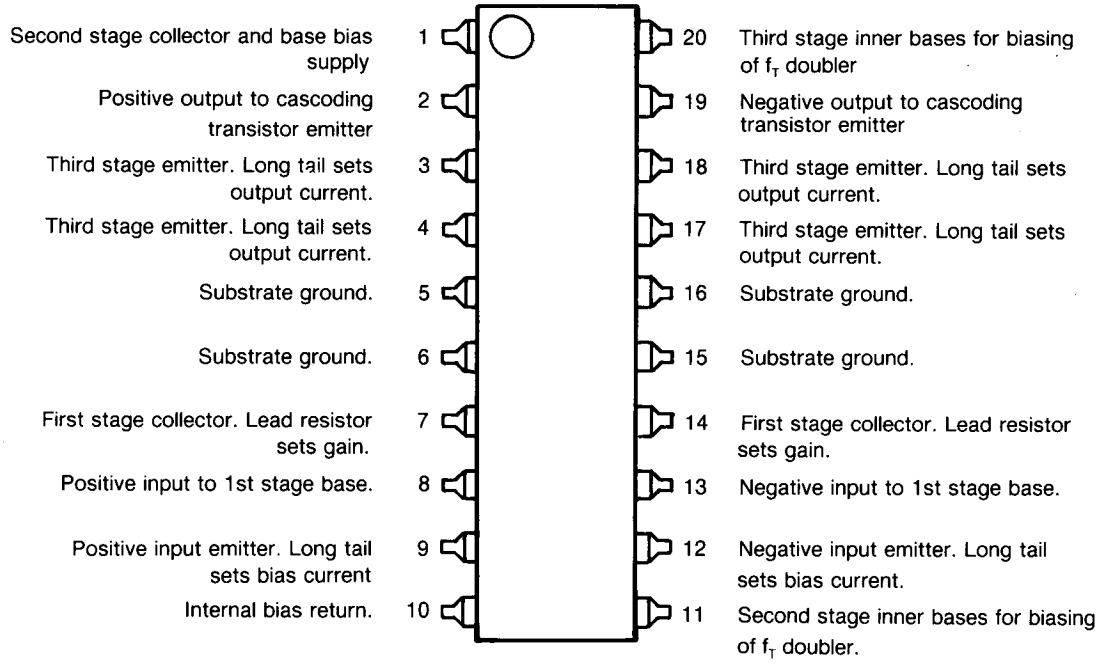
Currents are referenced positive into each port.

Pins 5, 6, 10, 15, and 16 are connected to circuit ground.

Unless otherwise designated, all voltages are referenced to circuit ground.

SYMBOLS	IDENTIFICATIONS	NOTES	MIN	MAX	UNITS
T_j	Junction temperature, operating		−15	+125	°C
T_{stg}	Storage temperature		−62	+125	°C
P_D	Total-device power dissipation, junction to case	Derate by 40 mW for each °C by which T5, 6, 15, 16 exceeds 25°C.		4.0	W
I_2 or I_{19}	Output emitter current.			80	mA
I_9 or I_{12}	Input collector current.			−40	mA
V_1	Internal supply voltage.			12.5	V
V_{CIO}	Collector to substrate voltage.	Any transistor.		30.0	V
V_{CBO}	Collector to base voltage.	Any transistor.		15.0	V
V_{CEO}	Collector to emitter voltage.	Any transistor.		5.0	V
V_{EBO}	Emitter to base voltage.	Any transistor.		4.0	V
I_C	Collector current.	Q1 through Q6 Q7 through Q14		80 40	mA mA
T_L	Lead temperature during soldering	≤10 sec		240	°C
θjc	Thermal resistance (junction to case)	Case temperature center tab temp.		25	°C/W

PACKAGING



ELECTRICAL CHARACTERISTICS

Unless noted otherwise, ambient temperature = 25°C.

Subscripts correspond to 155-0218-00 pin numbers. Pins 5, 6, 10, 15, and 16 are connected to ground.

PARAMETRIC DEFINITIONS

The following Parametric Summary is based on the application shown schematically in Figure 2. Recognize that this represents only one application. Other biasing arrangements are possible as long as the Absolute Maximum Ratings are not violated.

All currents are referenced positive into the device. Unless noted otherwise, voltages are referenced to ground.

ELECTRICAL CHARACTERISTICS

SYMBOL	NAME	NOTES	MIN.	TYP.	MAX.	UNITS
V_1	Internal supply voltage.			9.13		V
I_1	Internal supply current.			39.7		mA
I_2 or I_{19}	Output idle current.	$V_{in}+ = V_{in}- =$ 0 V	37	40.8	45	mA
$I_2 - I_{19}$	Output offset current	$V_{in}+ = V_{in}- =$ 0 V			4.1	mA
V_3, V_4, V_{17} or V_{18}	Third stage emitter voltage			7.91		V
V_7 or V_{14}	1st stage collector voltage			4.46		V
I_8 or I_{13}	Input bias current.	80 ≤ device β ≤ 200	40	65	100	μA
I_9 or I_{12}	Input emitter current	$V_{in}+ = V_{in}- =$ 0 V		−8.13		mA
V_{11}	Common mode bias voltage		3.9	4.1	4.3	V
I_{11}	Common mode bias current	80 ≤ device β ≤ 200		140		μA
V_{20}	3rd stage base voltage			7.91		V
I_{20}	3rd stage base current	80 ≤ device β ≤ 200		330		μA
$\frac{I_{19} - I_2}{(I_{in}+)-(I_{in}-)}$	Small signal differential current gain	$\lvert I_2\rvert - \lvert I_{19}\rvert = 0$ $\lvert I_2\rvert - \lvert I_{19}\rvert = 24.5$ mA	7.1	8.18 8.02	9.4	
$\frac{\text{Test 1-Test 2}}{\text{Test 1}}$	Small signal gain linearity	Corresponds to ± 3.5 div on screen.	0	−2	−3.5	%
T_r*	Risetime	In test fixture	0.5	1.0	2.0	ns

***This parameter is listed for characterization information only. It is NOT a production test. If new users seek guaranteed risetime for their application they must renegotiate this spec with ICM.**

APPLICATIONS INFORMATION

Application Aids

Refer to Figures 1 and 2 for the following discussion:

The input sensitivity of the amplifier is 1 mA/div differentially (+0.5 mA/div, −0.5 mA/div). Output current drive is nominally 8.18 mV/div differentially. Input emitters are exploited for DC balancing, delay line compensation, gain-temperature compensation and high speed "spiking" to overcome CRT plate RC rolloff. Adequate dynamic range, ±16 divisions first stage, ±14 divisions second stage and ±10 divisions 3rd stage is designed in to allow for the current overshoot with "spiking". Overall current gain is custom tailored by choice of input emitter resistance and 1st stage collector load resistance. Output quiescent current is programmed by choice of 3rd stage emitter resistor long tails. Thermal distortion is compensated in the third stage emitters. The op-amp automatically biases the 3rd stage f_T doubler.

Although designed for minimum power dissipation in a 100 MHz system, the part has sufficient margin in power dissipation capability to be derated at higher currents and voltages for higher bandwidth or higher performance applications. For example, V_{11} can be increased to provide higher VCE margins throughout the amplifier. In no case, however, should V_{11} nominally exceed 5.6 V or V_1 exceed 12 V. Output quiescent currents of up to 80 mA (I_2 or I_{19}) are available with a proper choice of 3rd stage emitter resistors.

Circuit layout for this part is CRITICAL. Input and output circuitry should be isolated from one another. Fortunately, this is facilitated by the location of the four grounded pins in the center of the part. Extensive ground plane should be run to and through the center of the part connecting to all four heat sinking pins. Ground plane should only be cut away beneath the input emitter circuitry 1st stage load resistors and output lines.

Package lead inductance is sufficient (particularly on the end pins) to require that any high speed input compensation be placed directly adjacent to the input end of the part. Similarly, the output cascode devices MUST be connected as directly as possible to the output (Pins 2 and 19).

Note that although case power dissipation is high, power dissipation is highly dependent on the leadframe to ambient thermal resistance.

2363 VERTICAL OUTPUT AMPLIFIER

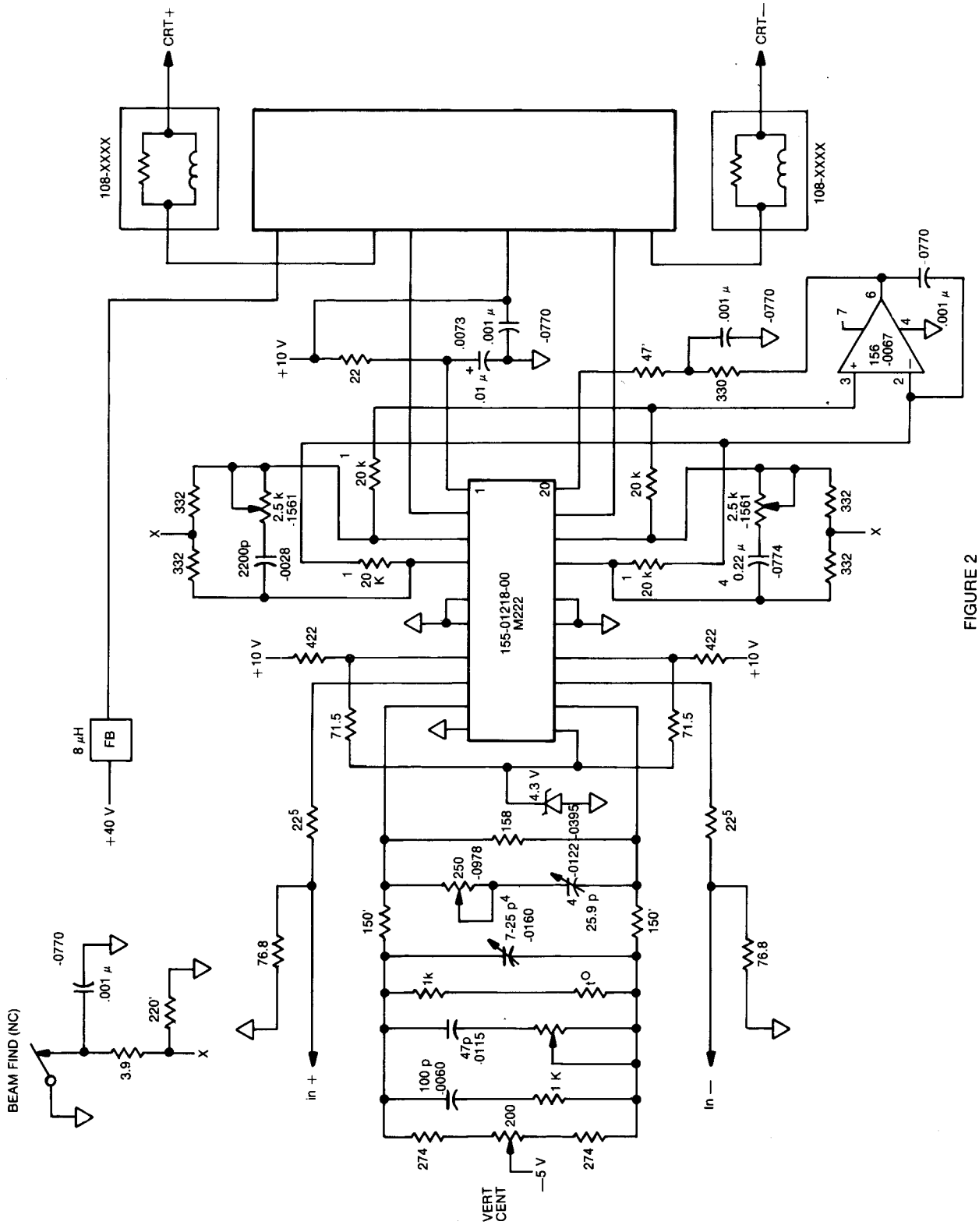


FIGURE 2

Product Precautions

Input Protection

A short to ground at package pins 3, 4, 17, and/or 18 will instantly destroy the component when it is under bias.

Reliability

Reliability Goal

λ, Failure rate $\leq$ 7.41%/1K hours at 150°C T_j.
λ, Failure rate $\leq$ .02%/1K hours at 75°C T_j.

Thermal Characteristics

The special leadframe (195-0072-02) used in this otherwise standard 20 pin DIP facilitates heat transfer from the die to the center four IC pins (Pins 5, 6, 15, 16). The temperature of the ground plane immediately adjacent to these pins must be controlled if the full power dissipation capability of the package is to be realized.

The part was characterized by using junction pulse techniques to measure junction temperature (Tj) while monitoring center leadframe temperature (Tc) at the point where it exits the plastic. θjc = 22°C/W.

5

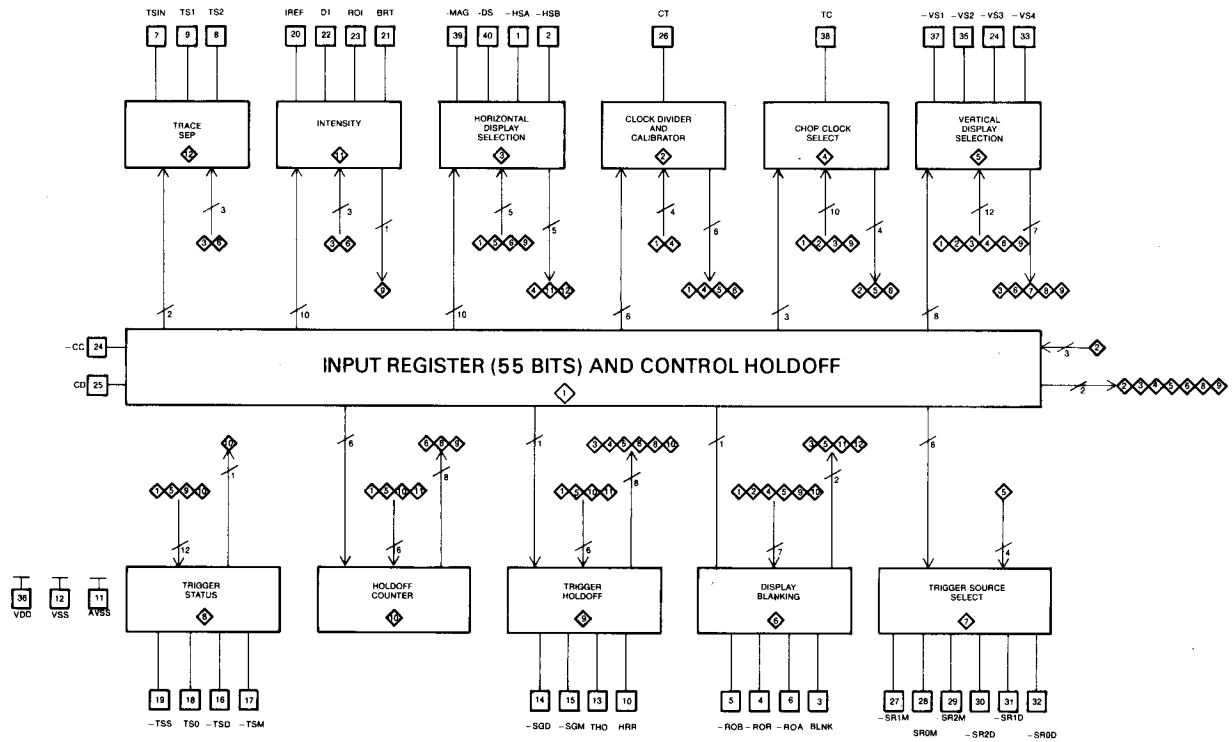
INTERFACE LOGIC

DESCRIPTION

The 155-0244-00 is a monolithic silicon (CMOS) device which is a display sequencer integrated circuit. This circuit implements real-time logic functions within an oscilloscope that are, in general, too fast or not appropriate for microprocessor implementation.

FEATURES

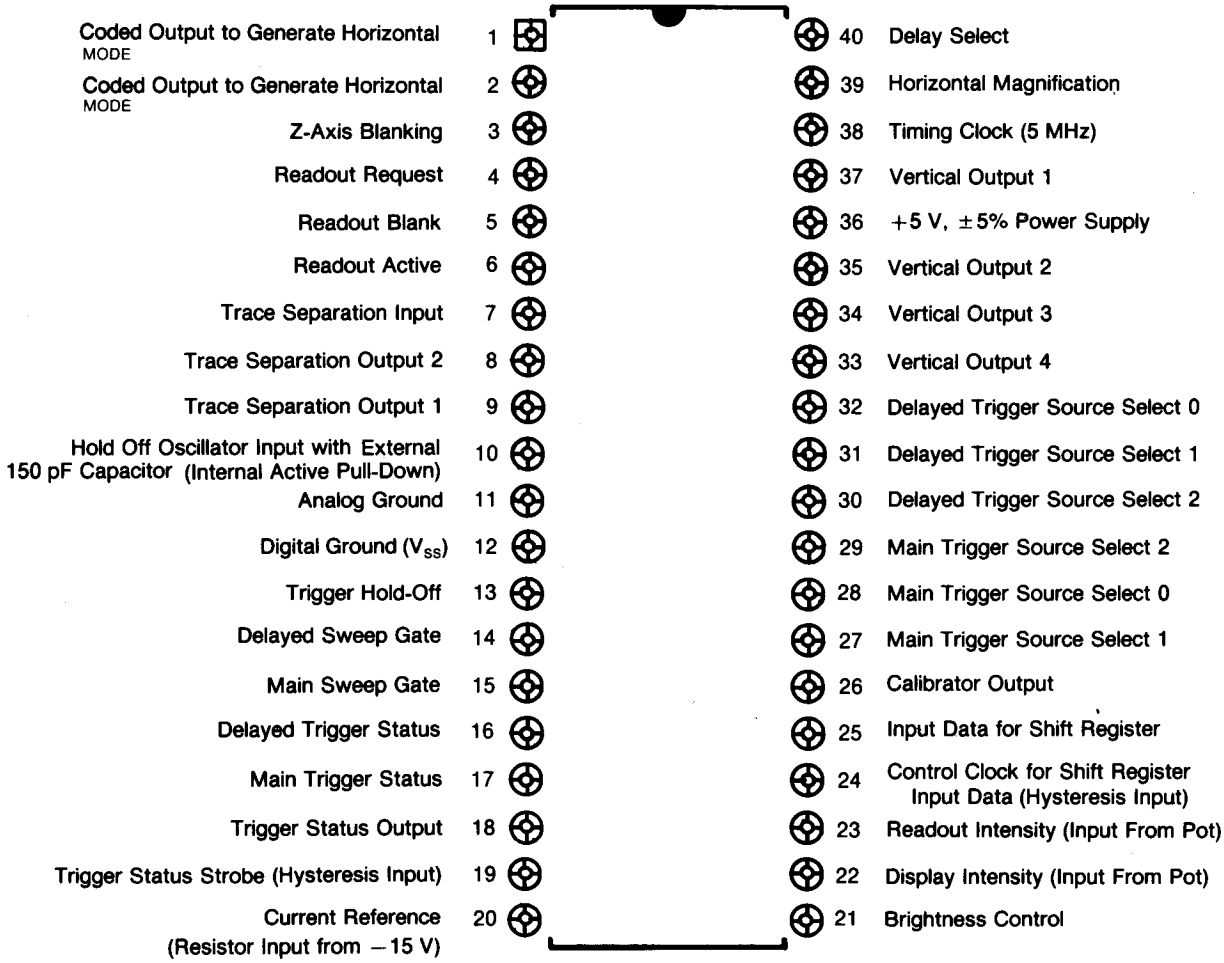
- Data is serially shifted from the μP. (55 bits)
- Clock divider divides down f_{clock} for use with chop clock, calibrator, and control holdoff.
- Horizontal display select.
- Vertical display select.
- Chop select.
- Display blanking.
- Trigger source select.
- Trigger status.
- Trigger holdoff.
- Holdoff counter.
- Display intensity.
- Trace separation.



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUES	UNITS
	Voltage on any pin relative to V_{EE}	−0.3 to V_{DD} +0.3	V
T_A	Operating Temperature (Ambient)	−15 to + 85	°C
T_S	Storage Temperature	−65 to +150	°C
P_D	Power Dissipation	0.1	W
T_j	Operating Junction Temperature	−15 to +90	°C

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
Voltage Supply (Operating)			
V_{SS} (ground)	Ground	Ground	
V_{DD} (+5 V nominal)	4.75	5.25	V
Static Power Dissipation			
F_{CLOCK} = 0 Outputs Open Circuit I_{DD}, current from V_{DD}		20.0	mA
Dynamic Power Dissipation			
F_{CLOCK} = 5 MHz C_L = 20 pF (all outputs) I_{DD}		25.0	mA

SYMBOL	PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
	Digital Inputs and Outputs			
V_{IH}	Input High Voltage (except −SGM and −SGD)	2.0	——	V
V_{IL}	Input Low Voltage	——	0.8	V
I_{IN}	Input Current	−10	+10	μA
V_{HYST}	Hysteresis Voltage on −CC and −TSS	0.1	——	V
I_{OL}	Output Low Current (V_{OUT} = 0.4 V)	1.6	——	mA
I_{OH}	Output High Current (except THO) (V_{OUT} = V_{DD}−.4 V)	——	−200	μA
I_{OH-THO}	Output High Current for THO (V_{OUT} = V_{DD} −.14 V)	——	−100	μA

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ELECTRICAL CHARACTERISTICS (cont)

SYMBOL	PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
	Analog Inputs and Outputs			
I_L	Leakage Current (off state)	−10	+10	μA
R_{INT}	Resistance to Bright from DI or ROI (V_{BRIGHT} = GND)	——	500	Ω
R_{TS1}	Resistance from TSI to TS1 TSI = 1.0 V I_{IN} = 100 μA	——	300	Ω
R_{TS2}	Resistance from TSI to TS2 TSI = 1.0 V I_{IN} = 100 μA	——	600	Ω
V_{REF}	Voltage at I_{REF} Input (I_{REF} = 160 μA)	400	900	mV
I_{DAC}	Current from MSB of DAC I_{REF} = 160 μA (Bright Output) (−200 mV < V_{out}) ≤200 mV	−685	−595	μA
I_{LIN}	Linearity of DAC Current	−17.5	+17.5	μA
V_{NOP}	Positive going threshold on HRR Input	2.5	3.5	V
V_{HON}	Negative going threshold on HRR Input	1.5	2.5	V
	Delay Times			
τ_{DV}	Delay from end of sweep to change in Vertical Outputs (V_{S1} − V_{S4})	——	150 + 3 T_{CLK}	nS
τ_{DV}	Delay from end of sweep to change in Horizontal Outputs (HSD, HSB, DS, MAG)	——	600	nS
T_{DVB}	Delay from change in Vertical Output to	——	50	nS
T_{DNVB}	Assertion/Deassertion Blanking during chop.	111	——	nS
τ_{DTS}	Delay from end of sweep to change in Trigger Source Outputs	——	200 + 2 T_{CLK}	nS
τ_{DTHO}	Delay from end of sweep to Assertion of THO	100	300	nS
τ_{DTSO}	Delay from −TSS to Valid Data on TSO	——	300	nS
τ_{SCD}	Valid Data Setup Time	300	——	nS
τ_{HCD}	Valid Data Hold Time	0	——	nS

ELECTRICAL CHARACTERISTICS (cont)

SYMBOL	PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
	Pulse Widths			
τ_{CLK}	Period of TC	200	——	nS
τ_{PW}	Positive or negative pulse width of TC	90	——	nS
τ_{SG}	Duration of Sweep Gates	50	——	nS
τ_{CB}	Chop Blanking Width τ_{CLK} = 200 nS		150	nS
τ_{SH}	Strobe High Width (TSS and CC)	700	——	nS
τ_{SL}	Strobe Low Width (TSS and CC)	300	——	nS
	Readout Timing			
	(−SGM to BLANK)— (SGM - HSX)	——	−30	nS
	(−SGM to VSX)— (−ROB to −BLANK)	——	280	nS
	(−SGM to −HSX)— (−ROB to −BLANK)	——	134	nS
	(ROB to BLANK) or (−ROB to −BLANK)	——	125	nS
	(ROB to BLANK)— (ROB to VSX) ROA Going False	——	34	nS
	(ROB to BLANK)— (ROB to HSX) ROA Going False	——	−39	nS
	(ROA to −THO)— (−ROA to VSX) ROA Going False	140	——	nS
	(ROA to −THO)— (−ROA to HSX) ROA Going False	286	——	nS
	Set-up time −ROB to −THO 2 Hock Mode	939	2000	nS
	Set-up time −ROB to −THO 2 Hock Mode Period = 1 μS	1500	2500	nS
	ROR to ROA	——	900	nS

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ELECTRICAL CHARACTERISTICS (cont)

SYMBOL	PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
	Readout Timing (cont)			
	(ROR to BLANK)— (ROR to VSX)	——	34	nS
	(ROR to BLANK)— (ROR to −HSX)	——	−39	nS
	(ROR to −VSX)— (ROB to −BLANK)	——	280	nS
	(ROR to −HSX)— (ROB to −BLANK)	——	134	nS
	(ROB to BLANK)— (−ROR · ROB to VSX)	——	34	nS
	(ROB to BLANK)— (−ROR · ROB to HSX)	——	−39	nS
	−BLANK to VSX −ROR · ROB Going True	140	——	nS
	−BLANK to HSX −ROR · ROB Going True	286	——	nS
	−ROR · ROB to −ROA	——	900	nS
	−ROR · ROB to BLANK $2\tau_{CLK}$	−100	$3\tau_{CLK+400}$	nS
	(−ROR to −BLANK)— (ROB to BLANK)	−100	+100	nS
	Settling Time—Analog Circuitry			
τ_{SB}	Settling Time to ±5 μA of Bright after change in Horizontal Select	——	500	nS
τ_{STS}	Settling Time to ±10 mV of TS1 or TS2 after change in Horizontal Select	——	300	nS

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APPLICATIONS INFORMATION

Input Register

Data is serially shifted into the 155-0244-00 from the μP. This data (55 bits) determines the functionality of 155-0244-00. Transitions of the control clock shifts data in, clears the divider chain, and initiates a signal "Control Hold-Off" that blanks the CRT and prevents triggering for at least τ_{CLOCK} X 10^3 after the last control clock goes high.

Clock Divider and Calibrator

Clock divider divides down f_{CLOCK} for use with chop clock, calibrator, and control hold-off. The calibrator gives a square wave output whose frequency is some multiple of f_{CLOCK}.

Horizontal Display Select

The two outputs HSA and HSB select one of four horizontal displays; DS selects one of two sweep delays; and Mag selects the horizontal amplification factor.

The horizontal display changes at the end of each Main Sweep.

In single sequence mode, each selected horizontal state is accessed once for each selected vertical state, then hold-off remains asserted until 155-0244-00 is updated by the system controller.

Vertical Display Selection

Four outputs from Vertical Display select drive inputs on the vertical channel switch, selecting one of the four vertical channels. The vertical display changes state at the end of the horizontal display sequence or at each positive transition of the chop clock.

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Chop Clock Select

This circuitry selects source of vertical clock for either chop or alternate mode.

Selects chop clock rate, varying between f_{CLOCK} and $\frac{f_{CLOCK}}{100{,}000}$

Adds one extra count to clock divider every sweep every other 50,000. Timing clock to provide skew in chop clock.

Display Blanking

Chop Blanking—Blank asserted for $\frac{\tau_{CLOCK}}{2}$ during transitions of vertical select when display being chopped.

Allows ROB input to control blanking during Readout.

APPLICATIONS INFORMATION (cont)

Provides blanking interval of approximately 400 nS at end of Readout, during which horizontal and vertical outputs are reasserted and allowed to settle for waveform display.

Generates ROA signal in response to ROR or end of sweep to indicate when the Readout is active.

Trigger Source Select

The trigger source is determined by three outputs: SROM, SR1M and SR2M.

The data on these outputs is identical to a three-bit code on the control register and is static except when the code is "111". At this time, the trigger sources dynamically follow the selected vertical display.

Trigger Status

Trigger status monitors the activity on the sweep and trigger inputs. This data is latched and then output in a serial fashion on command from the system controller.

Each time the input shift register is updated, or each time the data is read out, data is transferred from the primary latches to the storage latches, and the primary latches are cleared.

Main sweep gates are counted and read out along with the trigger status data.

One bit of the data indicates when the single sequence is completed.

Trigger Hold-Off

At the end of sweep, trigger hold-off (THO) is initiated by 155-0244-00. At the same time, an on-chip oscillator is started. After a programmed number of oscillations, THO ends.

Also at the end of sweep, readout is enabled, as indicated by ROA.

Hold-Off Counter

This counter counts up to 500,000 periods of the HO Oscillator for generating the programmable Hold-off time.

The last three decades of the counter are used to count sweep gates when the interval is less than 5000.

This sweep count is read by the controller along with trigger status data.

APPLICATIONS INFORMATION (cont)

Display Intensity

Display intensity multiplexes currents from the Display intensity and Readout intensity inputs onto the bright output.

It also adds current to the output from a 4 1/2-bit DAC during the display intensity interval.

Separate DAC's are included for main and delayed sweep.

Trace Separation

Two analog switches transfer a voltage from input TSIN to either outputs TS1 or TS2.

These signals drive the vertical output amplifier to provide up to ±5 divisions of offset.

APPLICATIONS INFORMATION (cont)

INPUT REGISTER BIT ORDER

Data shifts in with Bit 54 first, Bit 0 last

BIT	FUNCTION
0	MS10, Main Sweep Intensity Code LSB
1	MS11
2	MS12
3	MS13
4	MS14, Main Sweep Intensity Code MSB
5	DS14, Delayed Sweep Intensity Code MSB
6	DS13
7	DS12
8	DS11
9	DS10, Delayed Sweep Intensity Code LSB
10	TH4, Trigger Hold-off Code MSB
11	TH3
12	TH2
13	TH1
14	THO, Trigger Hold-off Code LSB
15	Extend Sweep Count Capacity
16	Delayed Ends Main
17	Display Blank
18	ATSO, Add Unit of Trace Separation During Horizontal Display State, HDS2 and HDS6
19	ATS1, Add Unit of Trace Separation During Horizontal Display State HDS6
20	ICT, Inhibit Chop While Triggerable
21	ICS, Inhibit Chop During Sweep
22	Single Sequence
23	Include Vertical Display State VDS1
24	Include Vertical Display State VDS2

APPLICATIONS INFORMATION (cont)

25	Include Vertical Display State VDS12
26	Include Vertical Display State VDS3
27	Include Vertical Display State VDS4
28	MX, Magnify X/Y Display
29	MD, Magnify Delayed Sweep Horizontal Display
30	MM, Magnify Main Sweep Horizontal Display
31	Include Horizontal Display State HDS1
32	Include Horizontal Display State HDS2
33	Include Horizontal Display State HDS3
34	Include Horizontal Display State HDS5
35	Include Horizontal Display State HDS6
36	Include Horizontal Display State HDS7
37	Slave Delta Time to First Two Included Vertical Display States
38	VTO, Vertical Display State Timing Code LSB
39	VT1
40	VT2
41	CSROM, Main Trigger Source Code LSB
42	CSR1M
43	CSR2M
44	CSROD, Delayed Trigger Source Code LSB
45	CSR1D
46	CSR2D
47	Counter Test
48	CPO, Calibration Period Code LSB

APPLICATIONS INFORMATION (cont)

49	CP1
50	CP2
51	CP3
52	CP4
53	CHL, Control Hold-Off Time Code LSB
54	CHM, Control Hold-Off Time Code MSB

PRODUCT PRECAUTIONS

Input Protection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is strongly advised that special handling precautions be taken to avoid application of any voltage higher than the maximum rated voltage to this high impedance circuit.

For the proper operations, it is recommended that all inputs and outputs be constrained as follows:

Inputs constrained to the range of $V_{SS} \leq V_{IN} \leq V_{DD}$.

Outputs constrained to the range of $V_{SS} \leq V_{OUT} \leq V_{DD}$.

Handling Procedures

All CMOS devices should be stored or transported in conductive material so that all exposed leads are shorted together. CMOS devices should NOT be inserted into the conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.

All CMOS devices should be placed on a grounded bench surface and the operator should be grounded prior to handling the devices. This is done most effectively by having the operator wear a conductive wrist strap.

Whenever handling a CMOS circuit, DO NOT WEAR ANY NYLON CLOTHING.

DO NOT insert or remove CMOS devices from test sockets with the power applied. Check all of the power supplies to be used for testing CMOS devices and be certain that there are no voltage transients present.

When any lead straightening or hand soldering is necessary, provide ground straps for the apparatus used.

APPLICATIONS INFORMATION (cont)

DO NOT exceed the maximum electrical voltage ratings specified.

Double check the test equipment setup for the proper polarity of the voltage BEFORE conducting parametric or functional testings.

Cold chambers using CO_2 for cooling should be equipped with baffles and devices MUST be contained on or in conductive material.

OPERATING TEMPERATURE RANGE

This component is tested at 25°C but is guaranteed to operate continuously, as specified, over −15°C to +85°C ambient temperature.

Junction temperatures are less than 5°C greater than the ambient temperature.

5

TAPE DRIVE CONTROLLER

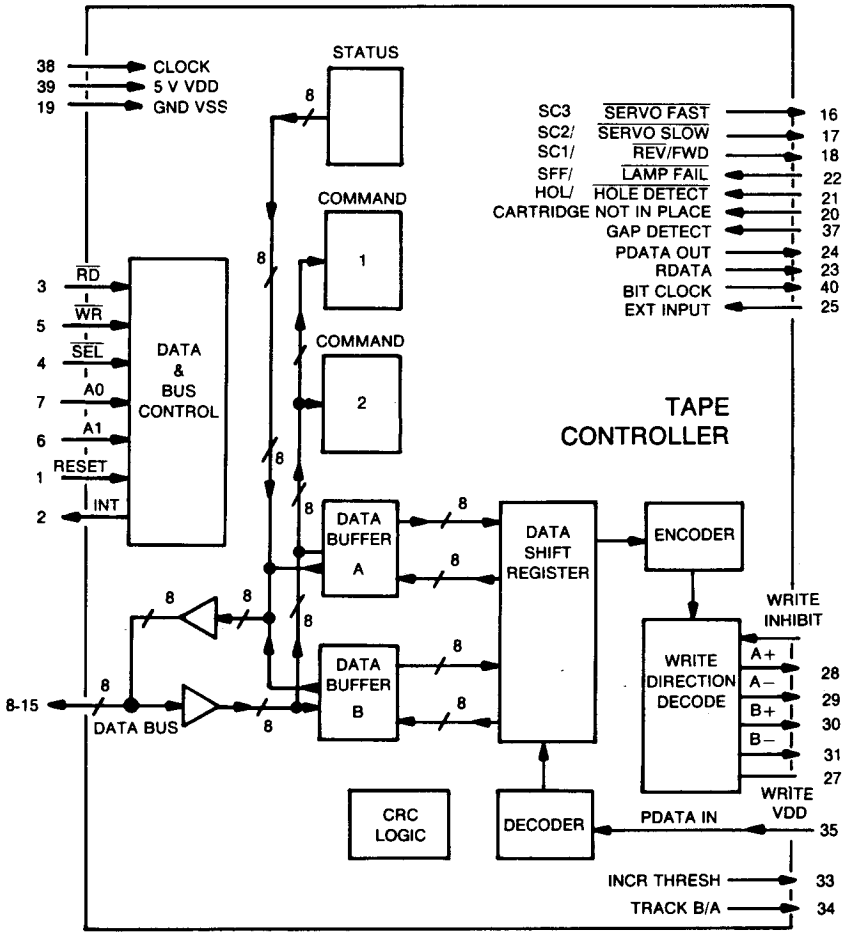
DESCRIPTION

The 155-0247-00 provides a means of interfacing a microprocessor to a data cartridge tape drive, with few external components. The tape controller receives control information and data from the processor in parallel form. The data is multiple buffered, serialized, encoded, then driven directly from the 155-0247-00 to the heads.

FEATURES

- Performs all drive data and control functions
- 32 kilobit/second operation
- Interrupt allows system multitasking
- On chip CRC—16 error detection
- 2 tracks selectable
- Compatible with current 8-bit microprocessors
- Users manual available by contacting Applications Engineering

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

Voltage on Any Pin Relative to V_{SS}	−0.3 V to +5.5 V
Operating Temperature, T_A (Ambient)	0°C to +60°C
Storage Temperature	−65°C to +150°C
Power Dissipation	0.2 Watt
Operating Junction Temperature, Tj	0°C to +70°C

PIN CONNECTIONS

ELECTRICAL CHARACTERISTICS

DC Parameters (V_{DD} = 5.0 V ±0.25 V, V_{SS} = 0.0 V)

Symbol	Identification	Min	Max	Units
V_{IH}	Input High Voltage (Except Clock)	2.0	——	Volts
V_{IL}	Input Low Voltage	——	0.8	Volts
V_{ICH}	Clock Input High Voltage	2.8	——	Volts
I_{IN}	Input Current	——	±10	μA
V_{OL}	Output Low Voltage at 2.4 mA Sink	——	0.4	Volts
V_{OH}	Output High Voltage at −100 μA Source*	2.4	——	Volts
I_{INTER}	Interrupt Output Current at 0.7 Volt	0.5	5	mA

*** This applies to Data Bus 0 to 7, Bit Clock, Rdata Out, Pdata Out, Track B/$\overline{A}$, and Increase Threshold Outputs. If Write V_{DD} = 5.0 ±0.25 V, this also applies to Write A+, Write A−, Write B+, Write B− outputs.**

Servo Fast, Servo Slow, and Reverse/Forward outputs are open for a logic 1 output.

AC Parameters

Symbol	Identification	Min	Max	Units
TCYC	Clock Cycle Time	950	10,000	nS
TCH	Clock High Time	450	———	nS
TCL	Clock Low Time	450	———	nS
TR	Clock Rise Time	0	100	nS
TF	Clock Fall Time	0	100	nS
TSS	Select Set-up Time	0	———	nS
TSH	Select Hold Time	0	———	nS
TAS	Address Set-up Time	50	———	nS
TAH	Address Hold Time	30	———	nS
TRDAC	Read Data Access Time	———	300	nS
TRDH	Read Data Hold Time	0	200	nS
TWR	Write Pulse Width	350	———	nS
TWDS	Write Data Set-up Time	130	———	nS
TWDH	Write Data Hold Time	30	———	nS

NOTE: All outputs are measured to standard V_{OL} and V_{OH} levels loaded with 100 pF to V_{SS}.

The reset pin is provided by the processor and must be held at a valid Logic One until after the V_{DD} supply reaches 4.75 volts. The input lines CNIP, HOLE DETECT, CAMP FAIL, GAP DETECT, WRITE INHIBIT, and PEAK DATA are assumed to be coming from a DC 100 tape drive and are very slow, asynchronous signals. Propagation delays through the 155-0247-00 are not defined.

APPLICATIONS INFORMATION

NOTE: In order to make use of this part in new designs, the following documents should be consulted:

155-0247-00 Tape Chip Users Manual

DC 100 Tape Drive Manual

The following information gives only a bare description of how the part is used.

Addressing

	A1	A0
Data Register	X	0
Command 1 Register	0	1
Command 2 Register	1	1
Status Register	X	1

Command and Status Register

COMMAND 1/ADDRESS 01

IT	TB/$\overline{A}$	R/$\overline{F}$	SS	SF	WRITE ($\overline{READ}$)	SYNC	SYNS

COMMAND 2/ADDRESS 11

ED1	ED2	EDS	GDA	WCO	CRCC	CRCS	CRCN

STATUS/ADDRESS 01

LF	HDET	CNIP	GDET	WINH —OVR	SYN	DS2	DS1

* * * * - can cause interrupts

Bit 7 Bit 0

EXPLANATION

Command 1

0-SYNS ..... Immediately strobes SYNC into SYN (Pulse)
1-SYNC ..... Intended Future Condition of SYN chronized
2-WRITE/$\overline{READ}$ ..... Intended Mode
3-SF ..... Motor Control Bit. Set to 00 by LF or HDET
4-SS ..... Motor Control Bit. Set to 00 by LF or HDET
5-R/$\overline{F}$ ..... Reverse or Forward Motor Direction
6-TB/$\overline{A}$ ..... Track B or A on Tape
7-IT ..... Increase Threshold OR Write Both Tracks

Command 2

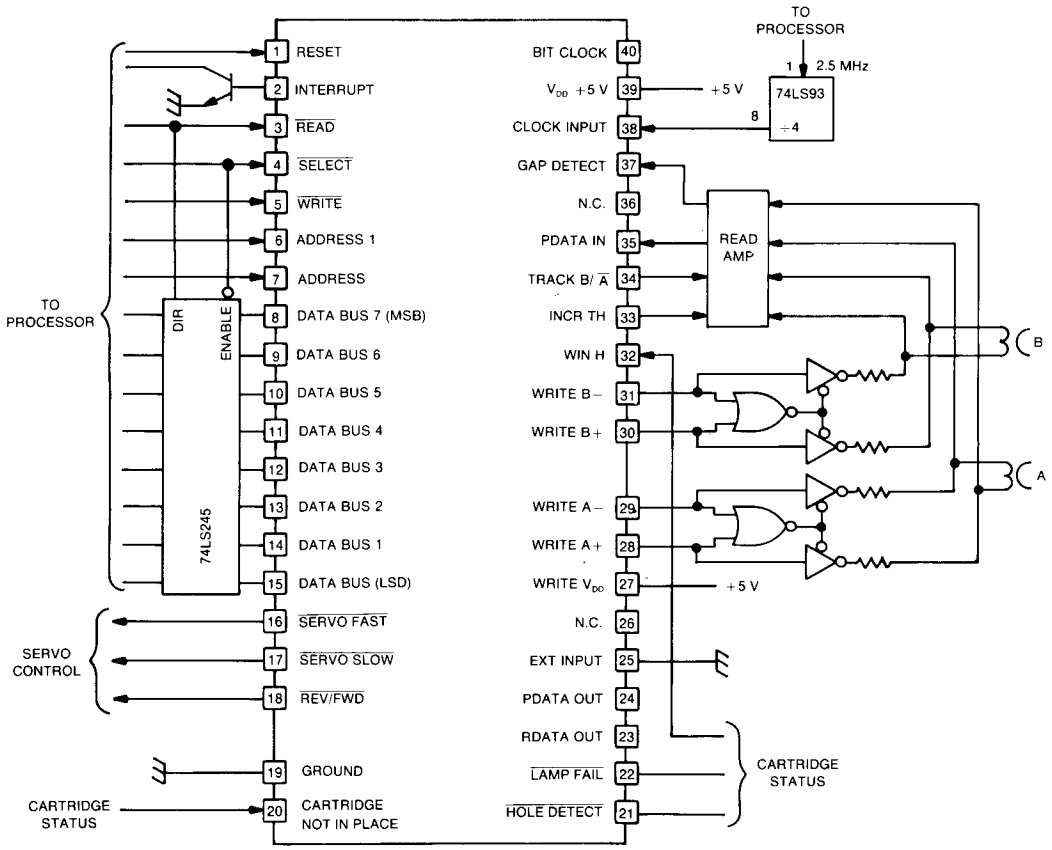
0 CRCN ..... Set CRC Mode Now (With CRCS) (Pulse)
1 CRCS ..... Set CRC Mode at Next SYNC Pulse (Pulse)
2 CRCC ..... Intended CRC mode—Changes after three data services
3 WCO ..... Write Current ON; For Writing Gaps
4 GDA ..... Gap Detect Interrupt Allow—Allows Tape Movement With or Without Gap
5 EDS ..... External Data Command Strobe (Pulse)
6 ED1 ..... External Data Command Bit 1
7 ED2 ..... External Data Command Bit 2

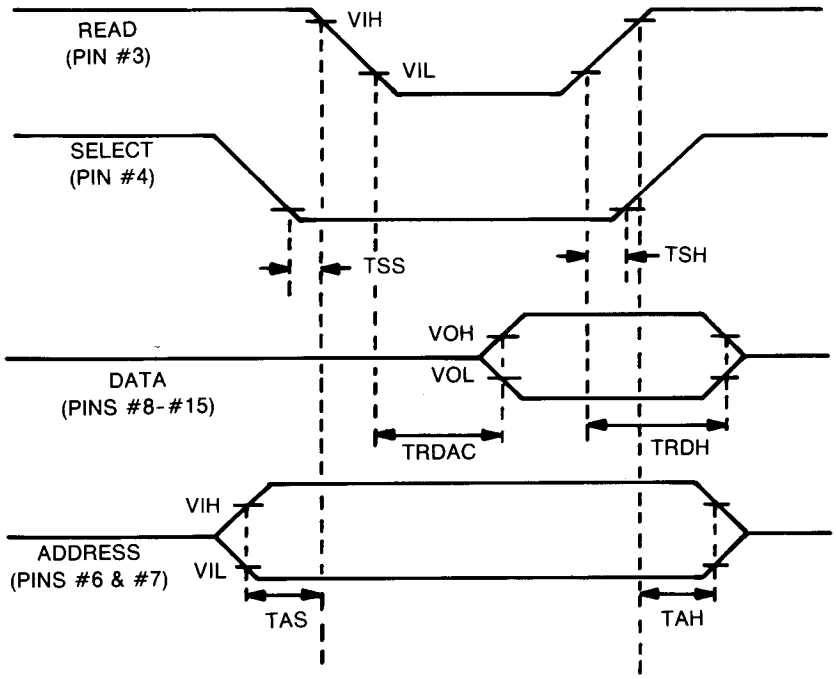
Status Register

0 DS1 ..... Indicates number of data services (Reads or Writes) necessary. 00, none; 01, 10, service once or twice; 11, overflow
1 DS2 ..... Indicates number of data services (Reads or Writes) necessary. 00, none; 01, 10, service once or twice; 11, overflow
2 SYN ..... Set if sync counter is running
3 WINH/OVR ..... Cartridge Write inhibit · $\overline{SYN}$ + Overrun · SYN
*4 GDET ..... Inter-record gap in tape data detected
*5 CNIP ..... Cartridge not in place
*6 HDET ..... Tape hole detected
*7 LF ..... Hold Detect Lamp Failure

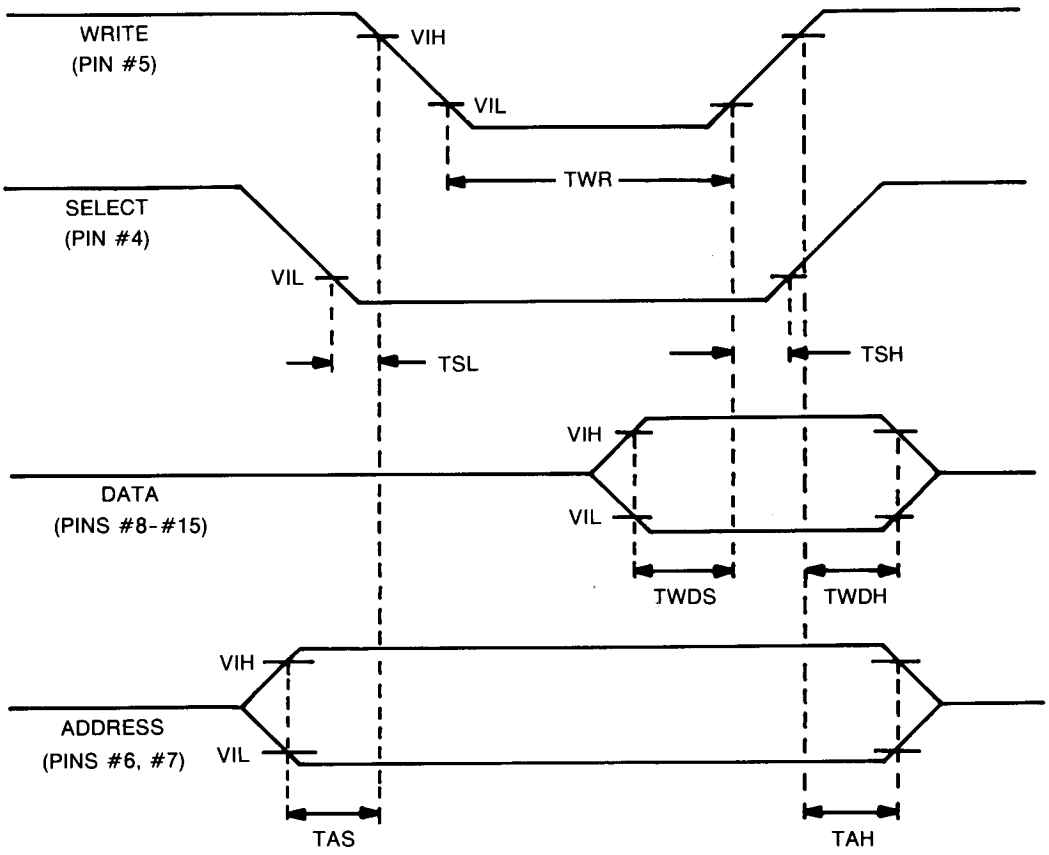
***Also: The DSI (data service interrupt) latches are set at each SYNC pulse, which also increments DS1 and 2.**

*** = Causes interrupts**





READ TIMING



WRITE TIMING

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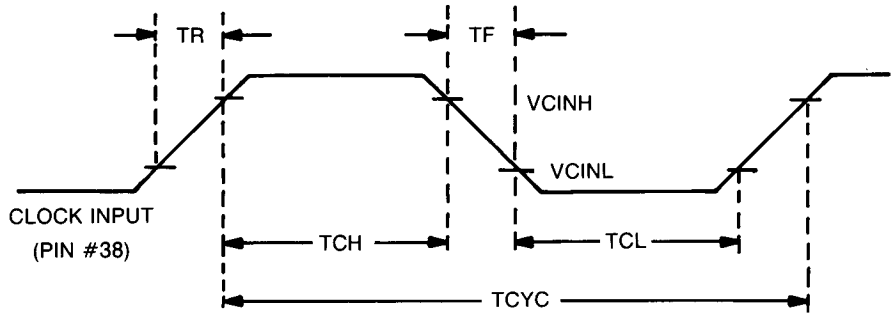


CLOCK TIMING

RELIABILITY

λ, Failure rate ≤ .1%/1K hours at 75°C Tj

Thermal resistance, die to case 25°C/W

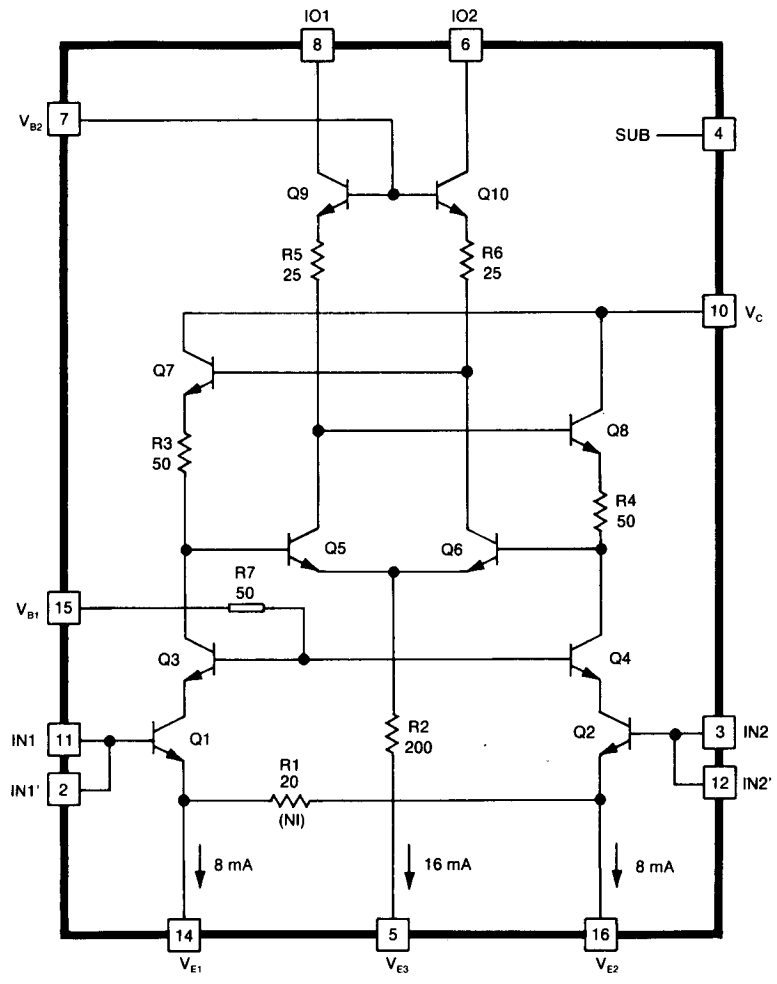
HIGH SPEED SCHMITT TRIGGER

DESCRIPTION

The 155-0253-00 is a high speed Schmitt trigger. The hysteresis and output current are adjustable. Accepts balanced or unbalanced input signals. Fabricated using the SH III process.

FEATURES

- 1.25 GHz
- Differential input and output
- Adjustable hysteresis and output current
- Trimmable gain resistor on die



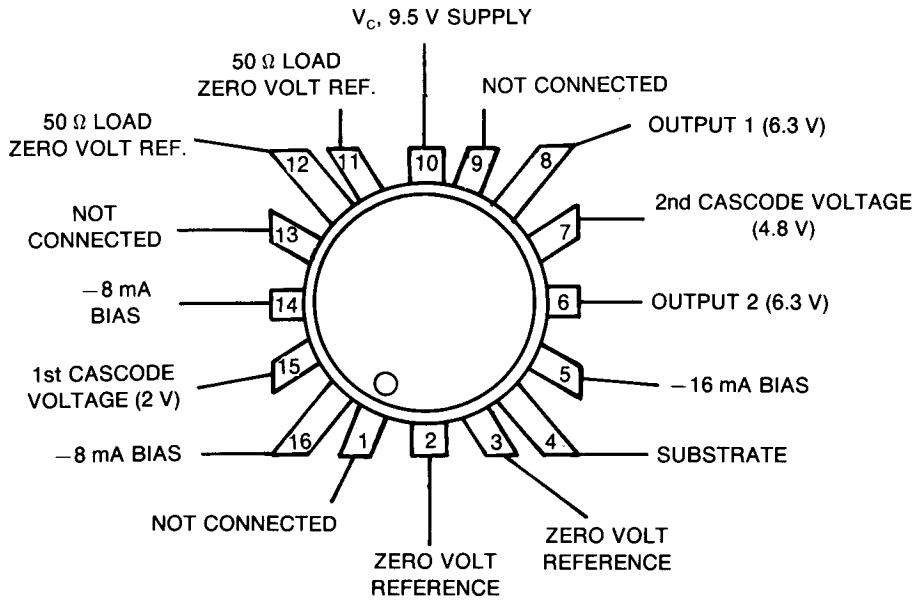
5

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUES	UNITS
T_{STG}	Storage Temperature	−55 to +125	°C
T_A	Operating Temperature	−15 to +70	°C Ambient
P_D	Power Dissipation (at 70°C)	270	mW
V_C	Supply Voltages	6	V
V_{IN}	Input Voltages	−1.0 to +1.0	V
	Bias Current I(14) or I(16) I(5)	 −8.0 −16.0	 mA mA
T_J	Maximum	120	°C

5

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER/CONDITIONS	MIN	MAX	UNITS
I_C	Supply Current, I into pin 10 at 9.5 V	14.5	16.8	mA
I_{B1}	First Cascode Bias Current I into pin 15 at 2.0 V	90	420	μA
I_{B2}	Second Cascode Bias Current I into pin 7 at 4.8 V	90	420	μA
I_1	Q1 Input Bias Current Measure I into pin 11 at 0.0 V	45	210	μA
I_2	Q2 Input Bias Current Measure I into pin 3 at 0.0 V	45	210	μA
I_{L1L}	Output 1 Lo Current Measure I into pin 8 at 6.0 V with pin 2: +400 mV pin 3: −400 mV			
I_{L2H}	Output 2 High Current Measure I into pin 6 at 6.0 V with pin 2: +400 mV pin 3: −400 mV	14.8	16.7	mA
I_{L1H}	Output 1 High Current Measure I into pin 8 at 6.0 V with pin 2: −400 mV pin 3: +400 mV	14.8	16.7	mA
I_{L2L}	Output 2 Low Current Measure I into pin 6 at 6.0 V with pin 2: −400 mV pin 3: +400 mV	0	20	μA
S	Sensitivity	139.4	200.6	mV
V_{OS}	Input Offset Voltage	−7	+7	mV

6.2 **Typical,* But Untested Performance Parameters**

The input sensitivity will be up 3 dB at 500 MHz. The circuit cannot be triggered past 1.25 GHz.

***NOT GUARANTEED**

APPLICATIONS INFORMATION

It is recommendd that pin 10 be well bypassed.

Pins 7 and 15 should have about 100 Ω resistance before bypassing.

PRODUCT PRECAUTIONS

Input Protection

Being a bipolar circuit, the 155-0253-00 is not particularly sensitive to static. However, care should be taken not to exceed any of the SHF-3 breakdown limits, especially BV_{EBO} and BV_{CBO} (4.5 V and 14 V, respectively).

Note that there is a short between pins 2 and 11 and also between pins 3 and 12. Application of an unlimited voltage source between these pins may destroy metal runs on the die.

Output Loading

Do not exceed the maximum output supply voltage (6 V) on pins 6, 8, and 10. Excessive voltage will cause excessive power dissipation.

Power Supply Turn-on/Turn-off Sequence

In order to prevent reverse biasing junctions, turn on the power supplies in the following sequence:

1. Substrate Voltage (pin 4)
2. Output Supplies (pins 6, 8)
3. VC (pin 10)
4. VB2 (pin 7)
5. VB1 (pin 15)
6. Bias Current

Turn off the power supplies in the reverse order of turn-on sequence.

Handling Procedure

The 16-pin Tek mini-pac is easily damaged by rough handling. The pins bend easily, and they pull out of the molded plastic body.

RELIABILITY

λ, Failure rate ≤.02%/1K hours at 75°C T_j
Thermal resistance, θjA 85°C/W

AMPLIFIER

DESCRIPTION

The 155-0273-00 is a monolithic integrated circuit originally designed as an Oscilloscope Vertical Amplifier.

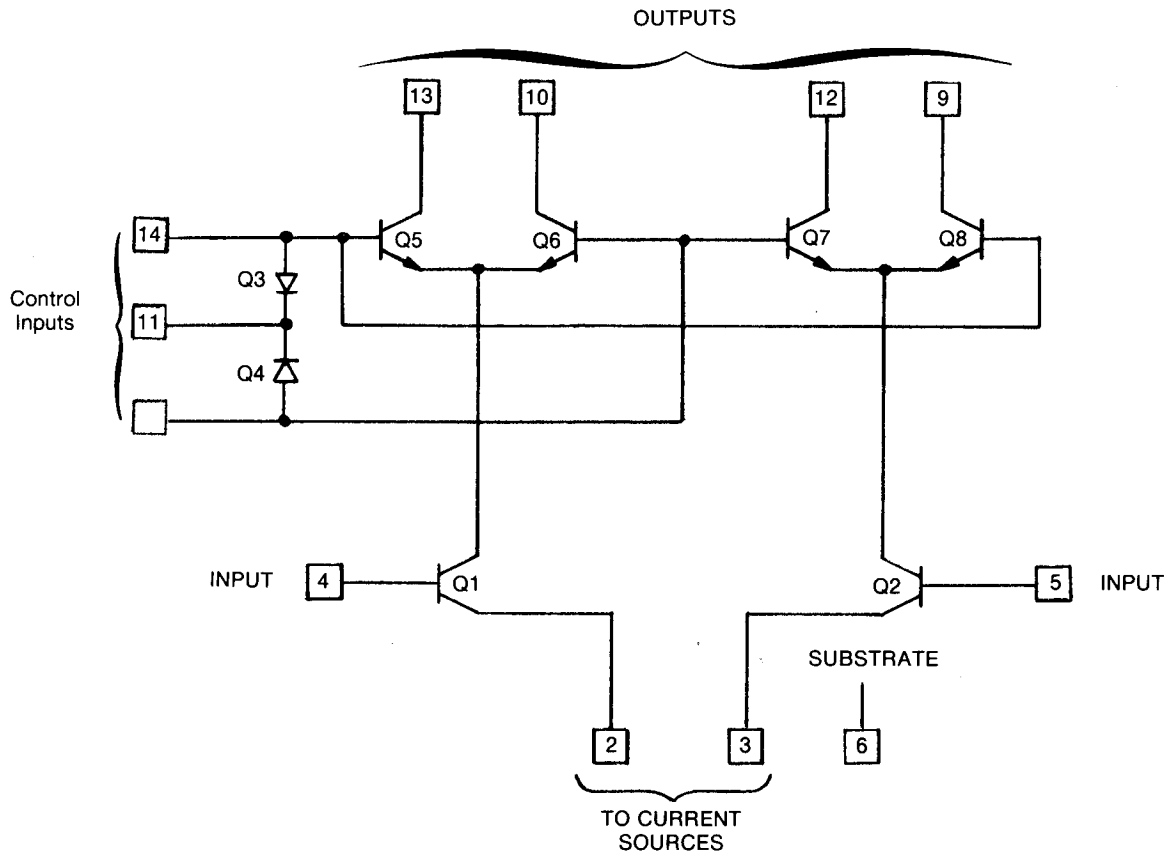
The circuit is a differential in, differential out amplifier with variable gain capabilities. By cross-coupling the output collectors, the circuit is basically a multiplier. DC voltages applied to the control inputs can be used to vary gain from the nominal (maximum) gain through zero to the negative nominal gain. Diodes are provided on the control inputs to linearize the gain characteristics.

FEATURES

- Nominal voltage gain set by external resistor.
- Gain variable from nominal (either polarity) to zero.
- Available in three versions:

  155-0078-10 (Minipak) (Fastest)
  155-0273-00 (14 pin DIP w/o nichrome resistors)
  155-0274-00 (14 pin DIP)

SCHEMATIC



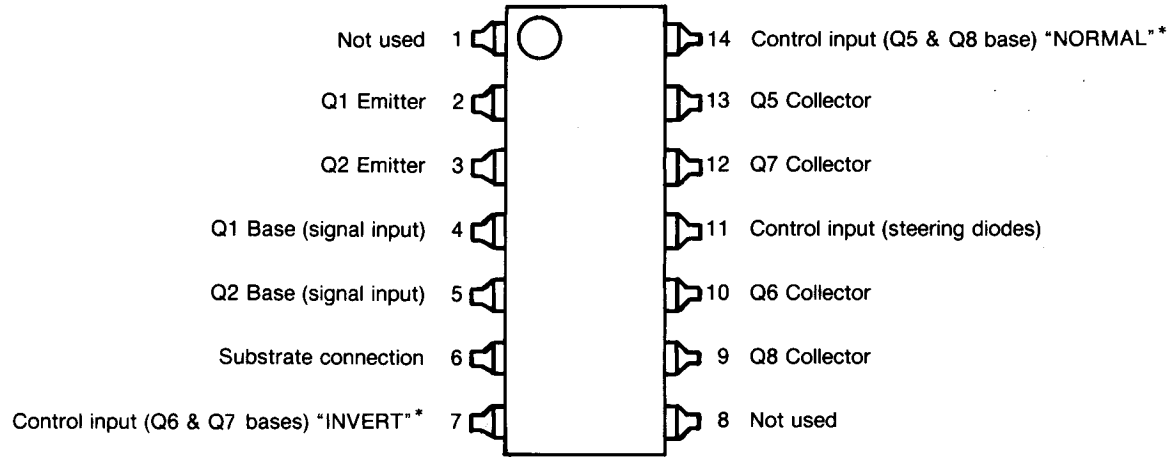
5

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	NOTES	VALUES	UNITS
$V_{out\text{-}sub\ MAX}$	Maximum voltage of the outputs (pins 13, 10, 12, 9) relative to the substrate (pin 6).	Prevents collector-substrate breakdown of Q5, Q6, Q7, Q8.	19	V
$V_{out\text{-}cont\ MAX}$	Maximum voltage of the outputs (pins 13, 10, 12, 9) relative to the control inputs (pins 7, 14).	Prevents collector-base breakdown of Q5, Q6, Q7, Q8.	7	V
$V_{cont\text{-}input\ MAX}$	Maximum voltage at the control inputs (pins 7, 14) relative to inputs (pins 4, 5).	Prevents collector-base breakdown of Q1 and Q2.	8	V
$V_{sub\text{-}input\ MAX}$	Maximum voltage of the substrate (pin 6) relative to the inputs (pins 4, 5).	Substrate voltage must be held more negative than any collector in circuit.	0	V
$V_{R03\ MAX}$	Maximum voltage from pin 11 to pin 7 or 14.	Maximum steering diode reverse voltage to avoid degradation.	2	V
$V_{R11\text{-}R12\ MAX}$	Maximum voltage from pin 7 to 14 or from pin 14 to pin 7.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
$V_{EB\ MAX}$	Maximum voltage from pin 2 to pin 4 or from pin 3 to pin 5.	Maximum base-emitter reverse voltage to avoid degradation.	2	V
I_{MAX}	Maximum current, pins 2 and 3.	Sum of pin 2 and pin 3 current.	36*	mA
P_{MAX}	Maximum power dissipation.	75°C ambient.	270	mW
$T_{OPERATING}$	Operating temperature range.		0 to 80	°C
$T_{STORAGE}$	Storage temperature range.		−55 to +125	°C
$T_{j\ MAX}$	Maximum junction temperature.		125	°C

*** Contact Applications Engineering, IC Manufacturing, if 20 mA is to be exceeded, pin 2 or pin 3.**

PIN CONNECTIONS



*Depends on polarity conventions—not indicated here.

ELECTRICAL CHARACTERISTICS

Specifications assume 32 Ω gain setting resistor (pins 2 to 3)

PARAMETER/CONDITIONS	MIN	MAX	UNITS
BV_{CEO} Q1, Q2, at 200 μA	4.4		Volts
BV_{CEO} Q5, Q6, Q7, Q8 at 200 μA	4.4		Volts
$BV_{CEO\ SUS}$ Q1, Q2 at 10 mA	4.9		Volts
$BV_{CEO\ SUS}$ Q5, Q6, Q7, Q8 at 10 mA	4.9		Volts
SUBSTRATE VOLTAGE in operating configuration		−15	Volts
INPUT BIAS CURRENT Q1 or Q2 (16 mA emitter current)	64	225	μA
NORMAL OFFSET	−14	+14	mV
INVERT OFFSET	−14	+14	mV
NORMAL GAIN	2.68	2.96	
INVERT GAIN	2.68	2.96	
NORMAL-INVERT GAIN MATCH	−0.5	+0.5	%
NULL OFFSET	−10	+10	mV
NULL GAIN	−.14	+.14	
50% GAIN	.49	.51	$X(AV_{NORM})$
OFF FEEDTHRU	−200	+200	μV

PARAMETRIC DEFINITIONS

The 155-0273-00 is specified in three different operating conditions: NORMAL, INVERT, and NULL.

In the NORMAL condition, Q5 and Q8 are conducting and Q6 and Q7 are not.

In the INVERT condition, Q6 and Q7 are conducting and Q5 and Q8 are not.

In the NULL condition, Q5, Q6, Q7 and Q8 are all conducting equally.

APPLICATIONS INFORMATION

Output Stage Considerations

Pin 7 and 14 can be voltage driven and pin 11 left open (Figure 1) if gain linearity as a function of control voltage is not critical. The voltage applied on pins 7 or 14 should be 1.2 to 3.7 volts above the quiescent voltage on pins 4 or 5 for conducting output transistors. For nonconducting output transistors pins 7 or 14 can be at a lower potential than this. Absolute maximum ratings must be observed, however. For the case of pin7 and 14 voltage driven and pin 11 open, gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{\exp\left(\frac{qV_{14}}{kT}\right) - \exp\left(\frac{qV_7}{kT}\right)}{\exp\left(\frac{qV_{14}}{kT}\right) + \exp\frac{(qV_7)}{kT}}\right]$$

where $A_{V\,NORM}$ = Normal Gain

V_7 = voltage applied on pin 7

V_{14} = voltage applied on pin 14

$\frac{kT}{q}$ = 26 mV at room temperature

If gain linearity as a function of control voltage is critical, pins 7 and 14 should be current driven and pin 11 returned to a voltage so as to set pins 7 and 14 voltage to the proper level as mentioned above. Figure 2 shows this type hookup. Current driving these inputs linearizes the gain by making use of the exponential current-voltage relationship of the diodes Q3 and Q4 to cancel that of the output transistors. The gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{I_{14} - I_7}{I_{14} + I_7}\right]$$

where I_7 = current into pin 7

I_{14} = current into pin 14

If variable gain of only a single polarity is desired, one pair of outputs can be used and the other pair connected to separate unused loads as in Figure 3.

If fixed maximum gain is desired, one pair of outputs can be left open as in Figure 4.

In applications where the output is to be switched from one output pair to another, the difference in offset voltage between the two outputs should not be spec'd any tighter than 28 mV (the sum of normal and invert offset specs).

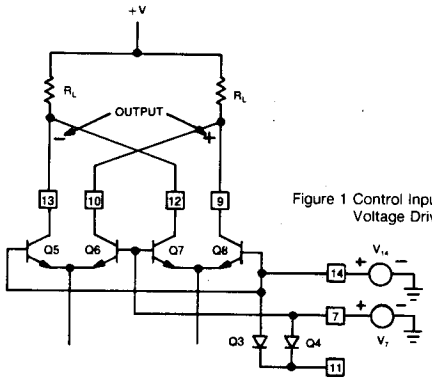


Figure 1 Control Inputs Voltage Driven

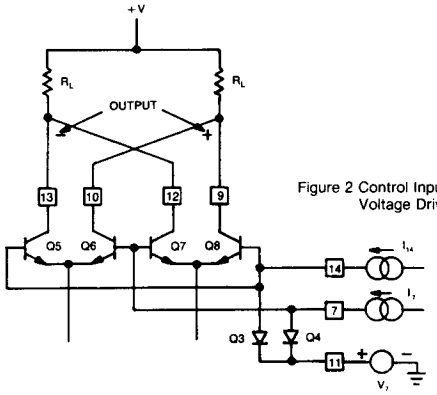
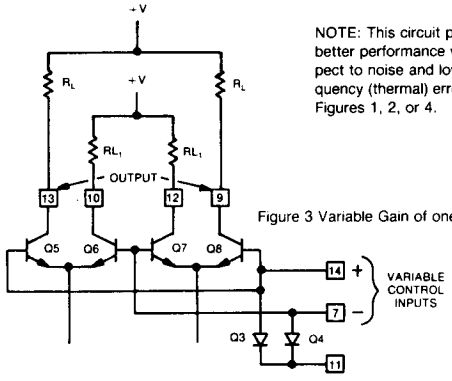
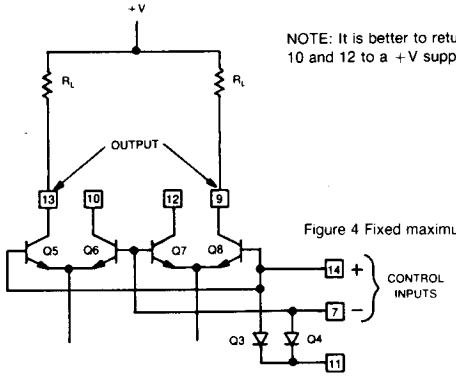


Figure 2 Control Inputs Voltage Driven



NOTE: This circuit provides better performance with respect to noise and low frequency (thermal) errors than Figures 1, 2, or 4.

Figure 3 Variable Gain of one polarity only



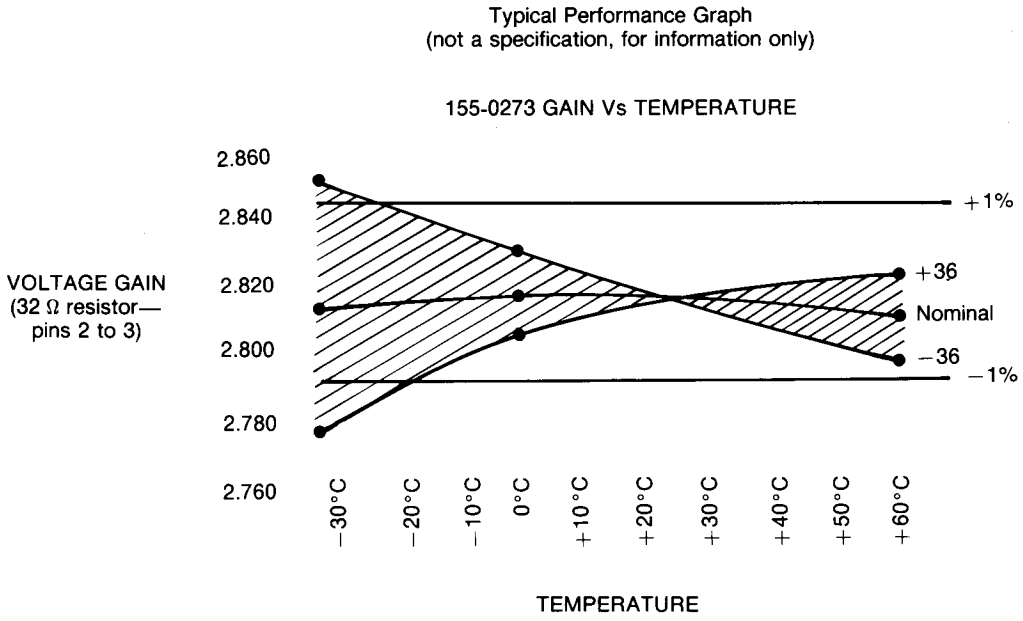
NOTE: It is better to return 10 and 12 to a +V supply if possible.

Figure 4 Fixed maximum gain

Input Stage Considerations

The bias current (pin 2 and 3 current) should not exceed 20 mA per side or a decrease in the life of the part may result.

Typical Performance Graph
(not a specification, for information only)



PRODUCT PRECAUTIONS

Input Protection

Input base-emitter voltages should not exceed 2 volts
in the negative direction and 1 volt in the positive direction.

Output Loading

Outputs should be limited to less than those listed in Absolute Maximum Ratings.

Power Supply Turn-On/Turn-Off Sequence

Substrate voltage should be turned on coincident with or before the other voltages.

Handling Procedures

Static sensitive handling procedures should be implemented for this part.

RELIABILITY

λ failure rate $\leq$ .025%/1K hours at 75°C Tj.

5

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AMPLIFIER

DESCRIPTION

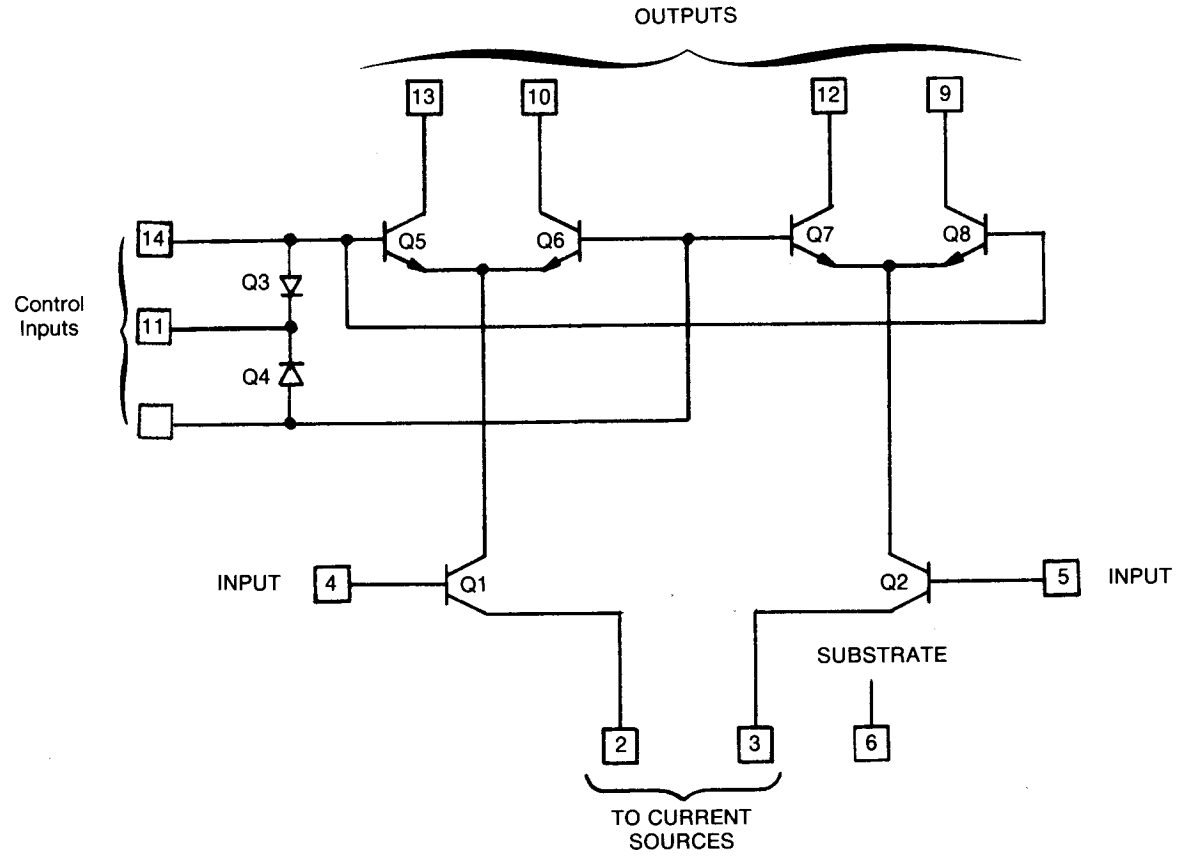
The 155-0274-00 is a monolithic integrated circuit originally designed as an Oscilloscope Vertical Amplifier.

The circuit is a differential in, differential out amplifier with variable gain capabilities. By cross-coupling the output collectors, the circuit is basically a multiplier. DC voltages applied to the control inputs can be used to vary gain from the nominal (maximum) gain through zero to the negative nominal gain. Diodes are provided on the control inputs to linearize the gain characteristics.

FEATURES

- Nominal voltage gain 2.82 (50 ohm source and loads). Set primarily by an on-chip nichrome resistor.
- Gain variable from nominal (either polarity) to zero.
- Available in three versions:
  155-0078-10 (Minipak) (Fastest)
  155-0273-00 (14 pin DIP w/o nichrome resistors)
  155-0274-00 (14 pin DIP)

SCHEMATIC



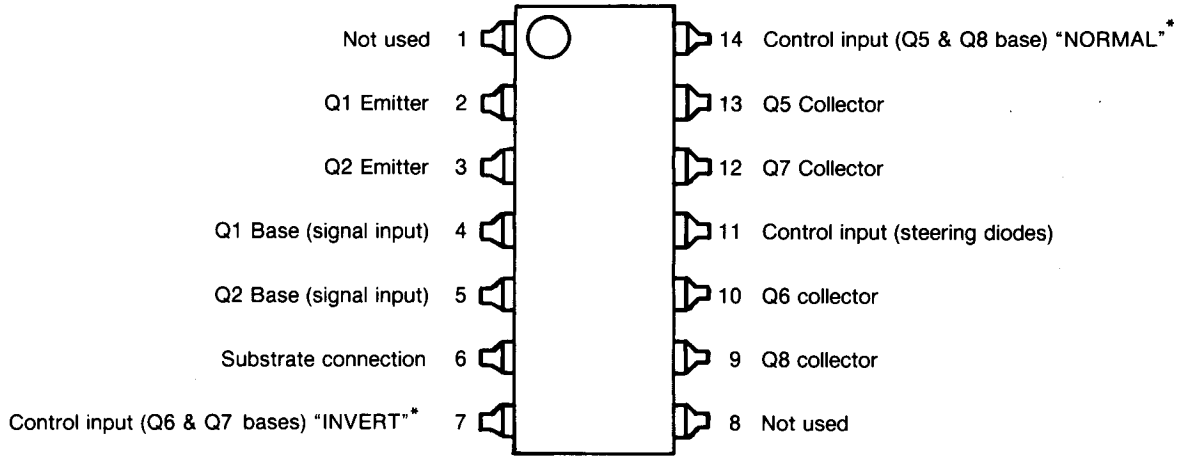
5

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	NOTES	VALUES	UNITS
$V_{out\text{-}sub\ MAX}$	Maximum voltage of the outputs (pins 13, 10, 12, 9) relative to the substrate (pin 6).	Prevents collector-substrate breakdown of Q5, Q6, Q7, Q8.	19	Volts
$V_{out\text{-}cont\ MAX}$	Maximum voltage of the outputs (pins 13, 10, 12, 9) relative to the control inuts (pins 7, 14).	Prevents collector-base breakdown of Q5, Q6, Q7, Q8.	7	Volts
$V_{cont\text{-}input\ MAX}$	Maximum voltage at the control inputs (pins 7, 14) relative to inputs (pins 4, 5).	Prevents collector-base breakdown of Q1 and Q2.	8	Volts
$V_{sub\text{-}input\ MAX}$	Maximum voltage of the substrate (pin 6) relative to the inputs (pins 4, 5).	Substrate voltage must be held more negative than any collector in circuit.	0	Volts
$V_{RQ3\ MAX.}$	Maximum voltage from pin 11 to pin 7 or 14.	Maximum steering diode reverse voltage to avoide degradation.	2	Volts
$V_{R11\text{-}R12\ MAX}$	Maximum voltage from pin 7 to 14 or from pin 14 to pin 7.	Maximum steering diode reverse voltage to avoid degradation.	2.5	Volts
$V_{EB\ MAX}$	Maximum voltage from pin 2 to pin 4 or from pin 3 to pin 5.	Maximum base-emitter reverse voltage to avoid degradation.	2	Volts
I_{MAX}	Maximum current, pins 2 and 3.	Sum of pin 2 and pin 3 current.	36*	mA
P_{MAX}	Maximum power dissipation.	75°C ambient.	270	mW
$T_{OPERATING}$	Operating temperature range.		0 to 80	°C
$T_{STORAGE}$	Storage temperature range.		−55 to +125	°C
$T_{J\ MAX}$	Maximum junction temperature.		125	°C

*** Contact Applications Engineering, IC Manufacturing, if 20 mA is to be exceeded for pin 2 or pin 3.**

PIN CONNECTIONS



*Depends on polarity chosen for inputs and outputs—Not indicated here

ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN.	MAX.	UNITS
BV_{CEO} Q1, Q2, at 200 μA	4.4		Volts
BV_{CEO} Q5, Q6, Q7, Q8 at 200 μA	4.4		Volts
$BV_{CEO\ SUS}$ Q1, Q2 at 10 mA	4.9		Volts
$BV_{CEO\ SUS}$ Q5, Q6, Q7, Q8 at 10 mA	4.9		Volts
SUBSTRATE VOLTAGE in operating configuration		−15	Volts
INPUT BIAS CURRENT Q1 or Q2 (16 mA emitter current)	64	225	μA
NORMAL OFFSET	−14	+14	mV
INVERT OFFSET	−14	+14	mV
NORMAL GAIN	2.68	2.96	
INVERT GAIN	2.68	2.96	
NORMAL-INVERT GAIN MATCH	−0.5	+0.5	%
NULL OFFSET	−10	+10	mV
NULL GAIN	−.14	+.14	
50% GAIN	.49	.51	X (AV_{NORM})
OFF FEEDTHRU	−200	+200	μV

PARAMETRIC DEFINITIONS

The 155-0274-00 is specified in three different operating conditions: NORMAL, INVERT, and NULL.

In the NORMAL condition, Q5 and Q8 are conducting and Q6 and Q7 are not.

In the INVERT condition, Q6 and Q7 are conducting and Q5 and Q8 are not.

In the NULL condition, Q5, Q6, Q7, and Q8 are all conducting equally.

APPLICATIONS INFORMATION

Output Stage Considerations

Pins 7 and 14 can be voltage driven and pin 11 left open (Figure 1) if gain linearity as a function of control voltage is not critical. The voltage applied on pins 7 or 14 should be 1.2 to 3.7 volts above the quiescent voltage on pins 4 or 5 for conducting output transistors. For nonconducting output transistors pin 7 or 14 can be at a lower potential than this. Absolute maximum ratings must be observed however. For the case of pin 7 and 14 voltage driven and pin 11 open, gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{\exp\left(\frac{qV_{14}}{kT}\right) - \exp\left(\frac{qV_7}{kT}\right)}{\exp\left(\frac{qV_{14}}{kT}\right) + \exp\left(\frac{qV_7}{kT}\right)}\right]$$

where $A_{V\,NORM}$ = Normal Gain

V_7 = voltage applied on pin 7
V_{14} = voltage applied on pin 14
$\frac{kT}{q}$ = 26 mV at room temperature

If gain linearity as a function of control voltage is critical, pins 7 and 12 should be current driven and pin 11 returned to a voltage so as to set pins 7 and 12 voltage to the proper level as mentioned above. Figure 2 shows this type hookup. Current driving these inputs linearizes the gain by making use of the exponential current-voltage relationship of the diodes Q3 and Q4 to cancel that of the output transistors. The gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{I_{14} - I_7}{I_{14} + I_7}\right]$$

where I_7 = current into pin 7
I_{14} = current into pin 14

If variable gain of only a single polarity is desired, one pair of outputs can be used and the other pair connected to separate unused loads as in Figure 3.

If fixed maximum gain is desired, one pair of outputs can be left open as in Figure 4.

In applications where the output is to be switched from one output pair to another, the difference in offset voltage between the two outputs should not be specified any tighter than 28 mV (the sum of normal and invert offset specifications).

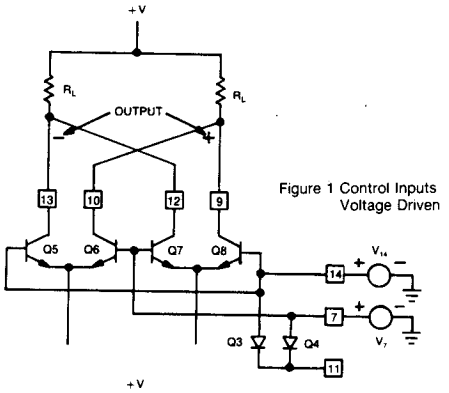


Figure 1 Control Inputs Voltage Driven

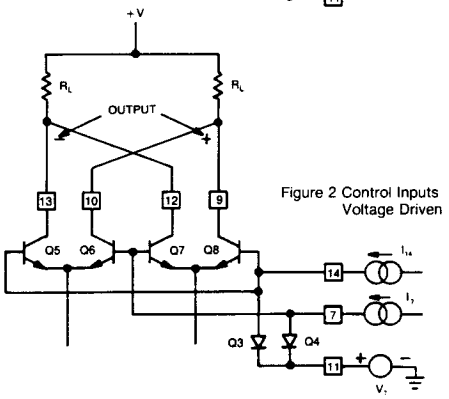
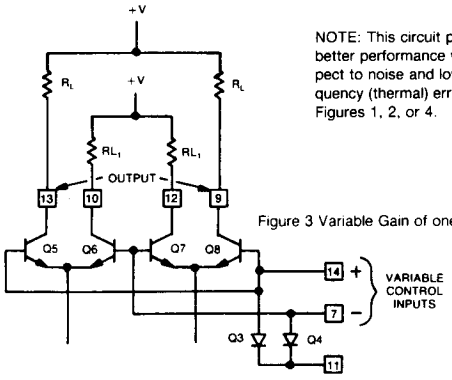
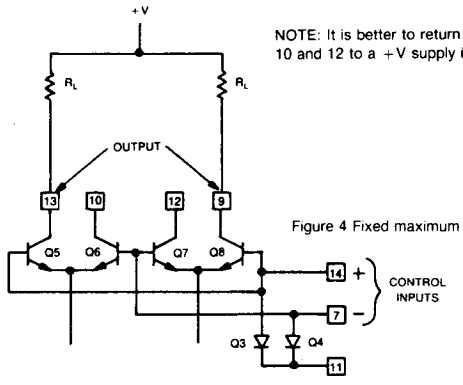


Figure 2 Control Inputs Voltage Driven



NOTE: This circuit provides better performance with respect to noise and low frequency (thermal) errors than Figures 1, 2, or 4.

Figure 3 Variable Gain of one polarity only



NOTE: It is better to return 10 and 12 to a +V supply if possible.

Figure 4 Fixed maximum gain

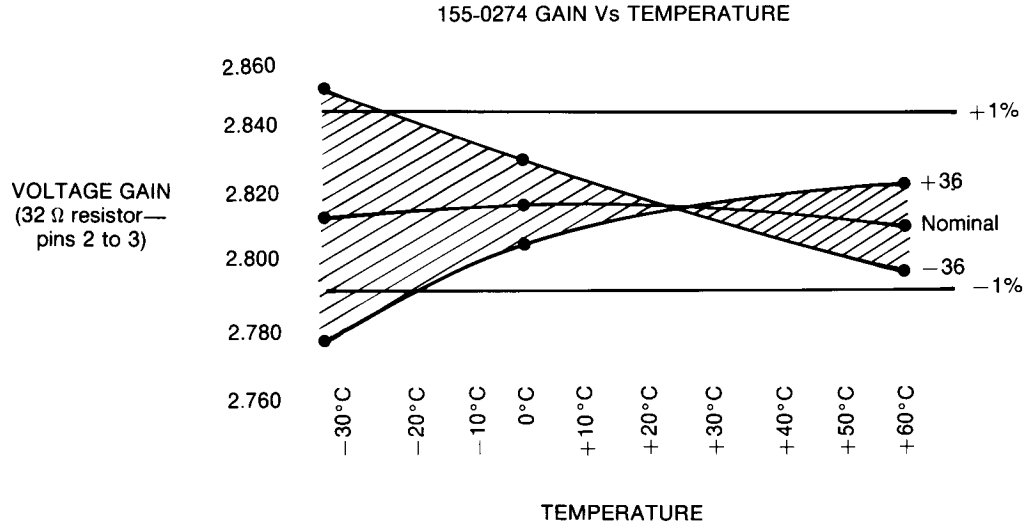
Input Stage Considerations

The bias current (pin 2 and 3 current) should not exceed 18 mA per side or a decrease in the life of the part may result.

Typical Performance Graph

(not a specification, for information only)

Typical Performance Graph
(not a specification, for information only)



PRODUCT PRECAUTIONS

Input Protection

Input base-emitter voltages should not exceed 2 volts in the negative direction and 1 volt in the positive direction.

Output Loading

Outputs should be limited to less than those listed in Absolute Maximum Ratings.

Power Supply Turn-on/Turn-Off Sequence

Substrate voltage should be turned on coincident with or before the other voltages.

Handling Procedures

Static sensitive handling procedures should be implemented for this part.

RELIABILITY

λ. failure rate $\leq$ .02%/1K hours at 75°C Tj.

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VIDEO MULTIPLIER

DESCRIPTION

The 155-0283-00 is a two quadrant analog multiplier/unity gain amplifier. Two signal inputs (Y, Z) and one gain/control input (X) are provided.

FEATURES

- ±10 V supplies
- Unity gain buffer function
- Two quadrant multiplier function
- 16 pin ceramic package
- 50 Ω Nichrome resistors

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUE	UNITS
T_J	Operating Junction Temperature	−15 to +125	°C
T_{STG}	Storage Temperature	−15 to +150	°C
VCC10	+10 V Supply	0 to +12	V
VEE10	−10 V Supply	−12 to 0	V
VIN (X, Y, Z)	Input Voltage	−2 to +2	V
RLoad	Output Load Impedance	2K to INF	Ω
CLoad	Output Load Capacitance	0 to 20	pF

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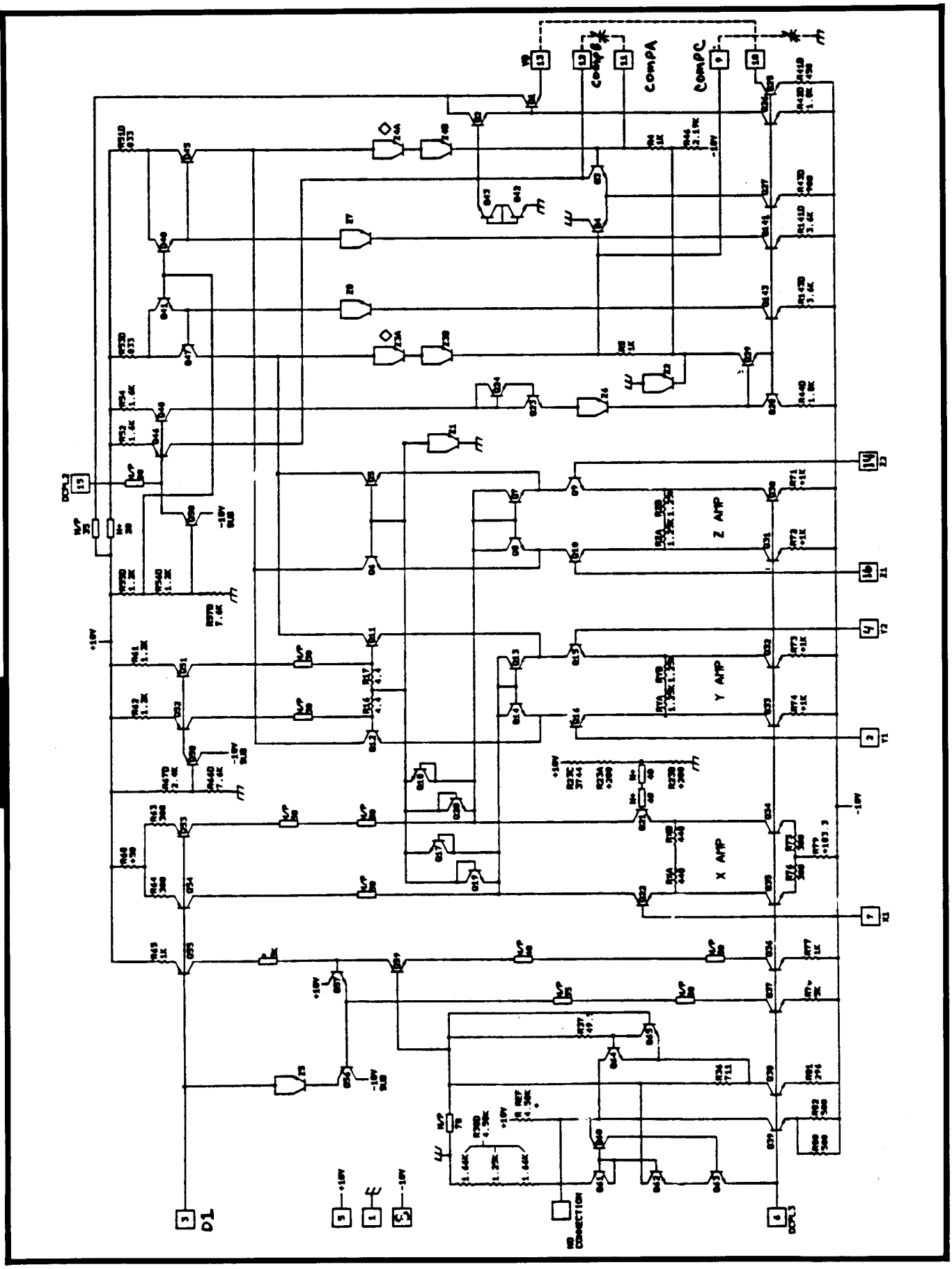
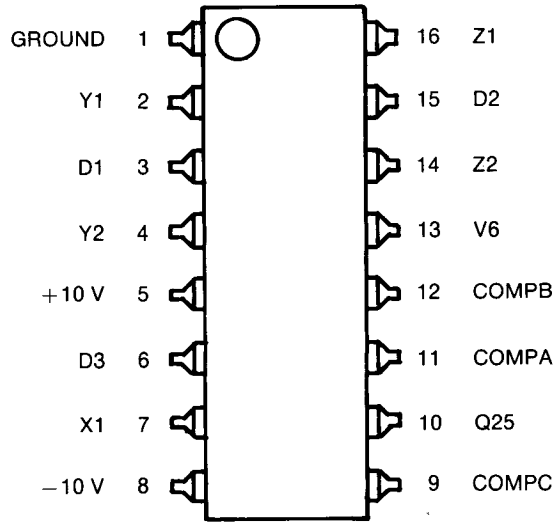

Z AMP
Y AMP
X AMP
CompB
CompA
CompC
-15V
+15V
CONNECTION

PIN CONNECTIONS

PIN #	NAME	INPUT/OUTPUT	DESCRIPTION
1	GND	Supply	Ground
2	Y1	Input	Y Video + Input
3	D1	——	Decoupling Capacitor
4	Y2	Input	Y Video − Input
5	+10 V	Supply	+10 V Supply
6	D3	——	Decoupling Capacitor
7	X1	Input	Control Input
8	−10 V	Supply	−10 V Supply
9	COMPC	——	External Compensation
10	Q25	Output	Q25 Output Collector
11	COMPA	——	External Compensation
12	COMPB	——	External Compensation
13	V6	Output	Q1 Emitter Output
14	Z2	Input	Z −Input
15	D2	——	Decoupling Capacitor
16	Z1	Input	Z +Input

PIN CONNECTIONS



5

ELECTRICAL REQUIREMENTS

NO.	SYMBOL	CONDITIONS	MIN	MAX	UNITS
1	——	10 V supply current	14.0	20.4	mA
2	——	−10 V supply current	−11.0	−17.6	mA
3	Zoffset	Z offset voltage X = −0.2 V Y = Z = 0 V	−5.0	5.0	mV
4	Yoffset	Y offset voltage X = 1.2 Y = Z = 0 V	−5.0	5.0	mV
5	BOW	X = .5 V, Y=Z=0 V BOW = Vo−(Yoffset + Zoffset)/2	−3.0	3.0	mV
6	——	Y Scale factor Δ Vo/.8 X = .1 to .9 V Z = 0 V, Y = 1 V	.98	1.02	——
7	——	Z scale factor Δ Vo/.8 X = .1 to .9 V Z = 1 V, Y = 6 V	−1.02	−.98	——
8	Zmic	Z midpoint X = .6 V Y = 0 V Z = 1 V	.485	.515	——
9	Ygain	Y follower gain X = 1.1 V, Z = 0 V Y = −1 V to +1 V Gain = Δ Vo/2	.997	1.003	——
10	Zgain	Z follower gain X = .1 V, Y = 0 V Z = −1 V to +1 V Gain = Δ Vo/2	.997	1.003	——

ELECTRICAL REQUIREMENTS (cont)

NO.	SYMBOL	CONDITIONS	MIN	MAX	UNITS
11	Yshift	Y shift X = 1.1 V Y = Z = 0 V Measure COMPC pad voltage.	−12.0	12.0	mV
12	Zshift	Z shift X = −.1 V Y = X = 0 V Measure COMPC pad voltage.	−12.0	12.0	mV
14	——	Input clipping level X = 0.1 V Y = 0.2 V	 1.0 2.0		 V V

RELIABILITY

Failure rate	0.02%/1000 hrs.
Reference junction temperature	75°C
Activation energy	1 eV

5

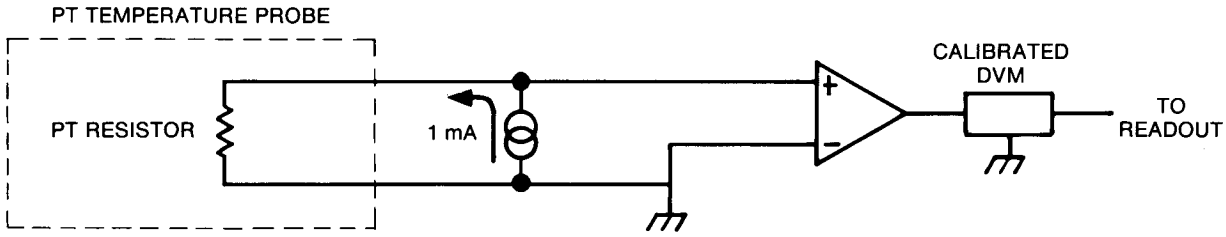
PLATINUM TEMP PROBE

DESCRIPTION

The platinum temperature probe utilizes a 100 Ω temperature sensitive resistor produced by depositing a platinum film on an oxidized wafer.

FEATURES

- 100 Ω ± .2 Ω at 0°C
- Resistance changes ~ .37 Ω/°C
- Laser Trimmed
- −70 to +240°C temperature range
- Withstands 1000g shock



ABSOLUTE MAXIMUMS

Electrical

Maximum Current Through Resistor	10 mA
For Accurate Measurements	<2 mA
Maximum Temperature, Operating	240°C
Maximum Temperature, Storage	120°C

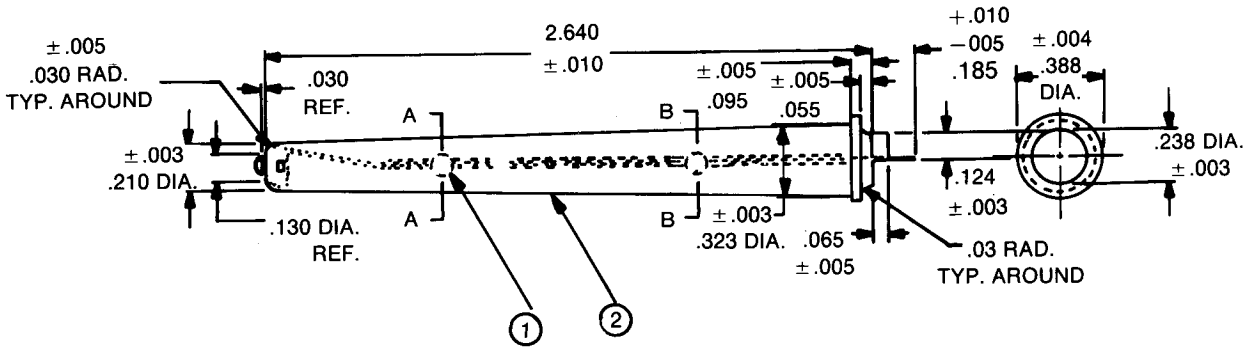
Environmental

The 206-0248-03 MUST NOT be immersed in any liquids incompatible with the following materials: Morton 410BSG and Beryllium Oxide (BeO).

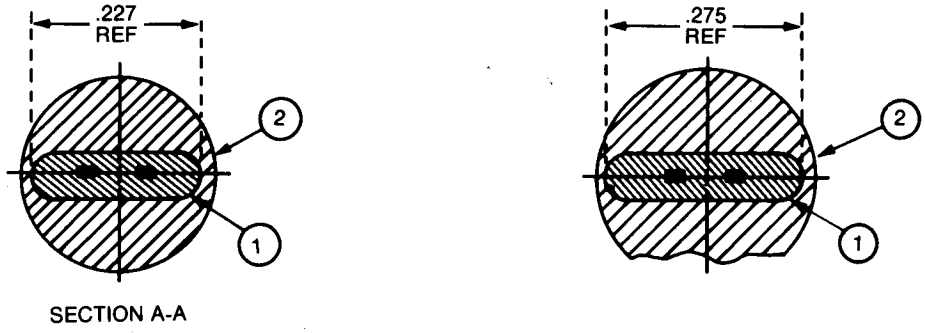
Mechanical

Maximum Axial Force	20 lbs
Maximum Normal Force	20 lbs
Axial Impact	1 ft-lb
Normal Impact	0.3 ft-lb
Shock	1000 g's, 1/2 sine, 5 mS, 1 mS, and 2 mS duration, 3 shocks, each axis, 18 total

PACKAGING



PACKAGING



SECTION A-A

PARAMETRIC SUMMARY

PARAMETER/CONDITIONS	MIN	MAX	UNITS
Input Current	——	10	mA
Temperature Range	−70	+240	°C
Temperature, Storage	−55	+120	°C
Altitude—Operating Storage		15,000 15,000	ft ft

DEFINITIONS

The "functional relationship of resistance with temperature" is defined by the boundary conditions of:

$R_T = 100\ (\pm\ .2\%) + .3700\ t\ (\pm\ .8\%) - 8.900\ (\pm\ 12\%) \cdot 10^{-5}t^2$

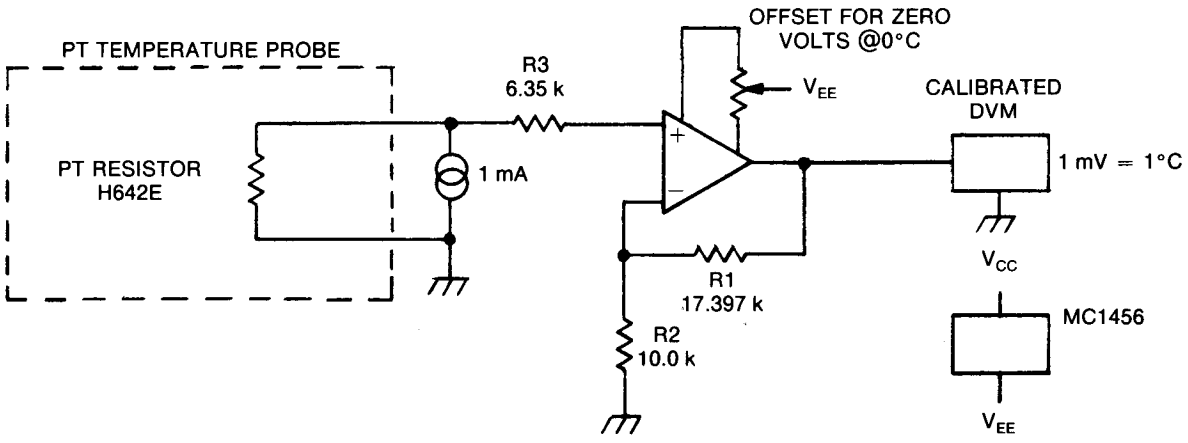
over the specified operating range.

The probe is to have a "resistance" equal to 100 Ω ± .2 Ω at 0°C.

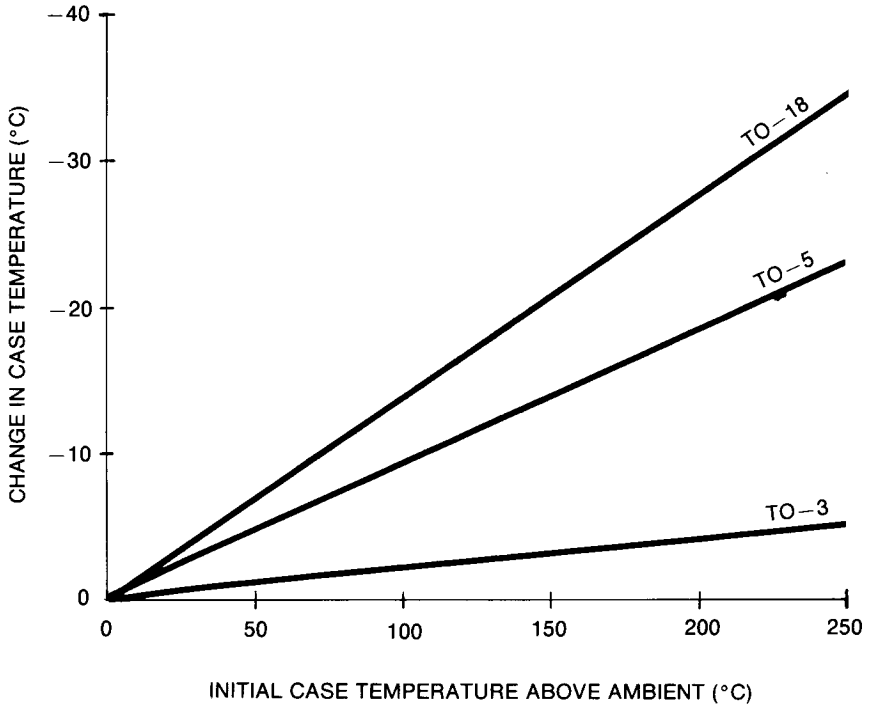
Temperature as a function of resistance may be determined by:

$T_R = -251.449 + 2.3252 \cdot R + 1.89 \cdot 10^{-3} \cdot R^2$

APPLICATIONS INFORMATION



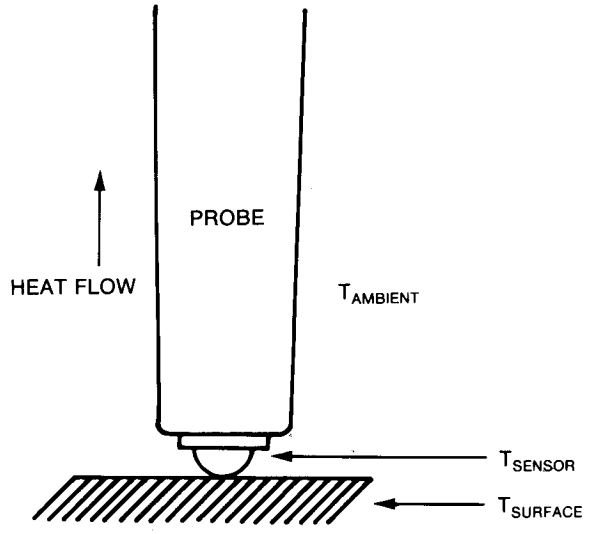
NOTE: **The above circuit is NOT the only circuit in which the Pt Temperature Probe will perform as a temperature measuring device. This circuit is shown only to give a reasonable idea of circuit complexity needed for calibrated probe operation.**



Typical decrease in device case temperature due to probe heat-sinking effect on various case sizes.

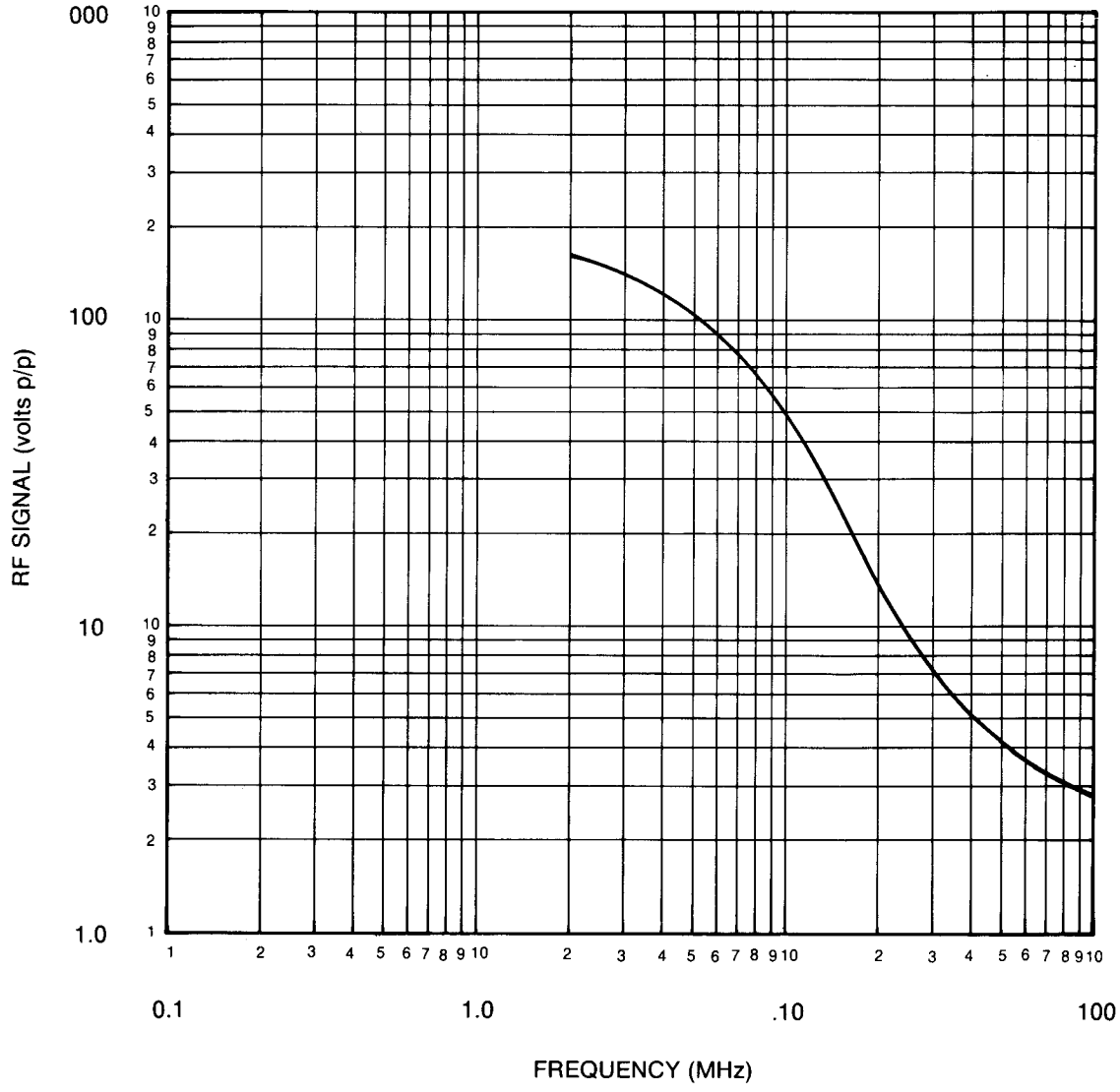
5

$$T_{SENSOR} - T_{AMBIENT} \approx 97.9\% \, (T_{SURFACE} - T_{AMBIENT})$$

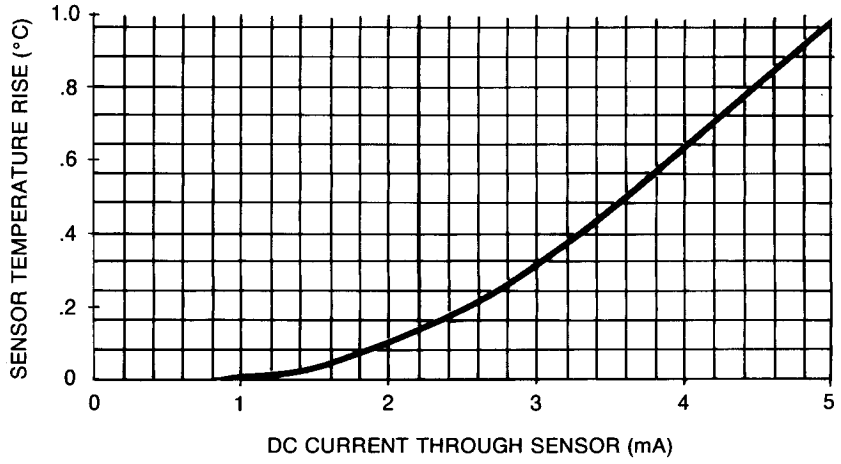


THERMAL GRADIENT EFFECT ON TEMPERATURE MEASUREMENT

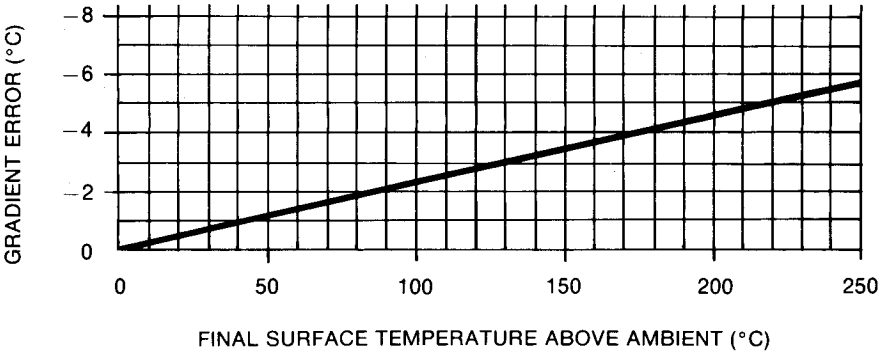
Thermal gradient is a "steady state" error that occurs when measuring the surface temperature, and is caused by the steady state gradient associated with the flow of heat from the surface being measured to the main probe body. Thus the temperature of the sensor will differ from the final surface temperature. This steady state error is dependent upon the final surface temperature above ambient. Naturally, this error does not occur when the entire probe is elevated to the temperature being measured.



Typical allowable rf signal limits at the probe tip



Self heating. Rise in sensor temperature due to instrument sensing current (at ambient = 25°C).



DIE (DATA SHEETS)

6

Page No.

SECTION 6 DIE (DATA SHEETS)

AMPLIFIER DIE

DESCRIPTION

The 203-0084-90 is an integrated circuit orignally designed as an Oscilloscope Vertical Amplifier.

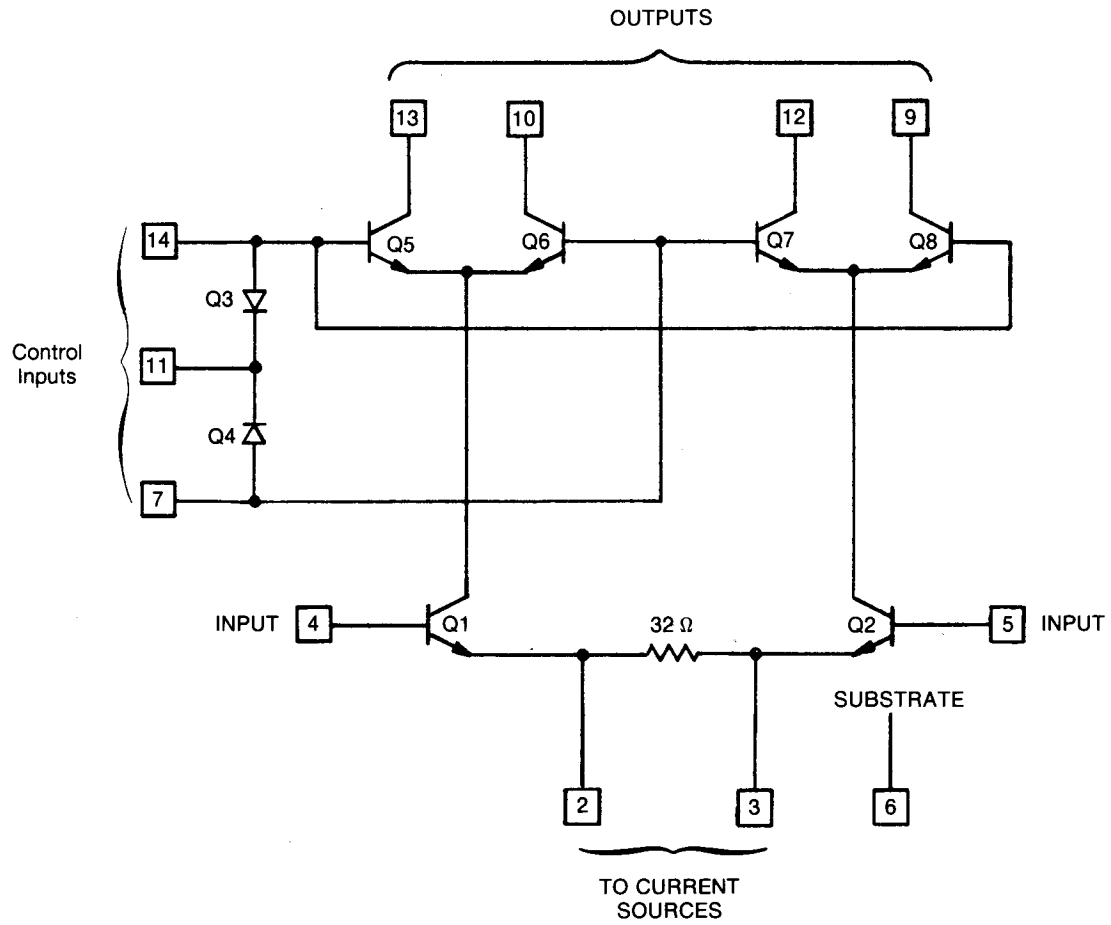
The circuit is a differential in, differential out amplifier with variable gain capabilities. By cross-coupling the output collectors, the circuit is basically a multiplier. DC voltages applied to the control inputs can be used to vary gain from the nominal (maximum) gain through zero to the negative nominal gain. Diodes are provided on the control inputs to linearize the gain characteristics.

FEATURES

- Nominal voltage gain 2.82 (50 Ω source and loads). Set primarily by an on-chip nichrome resistor.
- Gain variable from nominal (either polarity) to zero.
- Nominal bandwidth.
- Available in three versions:

  155-0078-10 (Minipak)
  155-0273-00 (14 pin DIP w/o nichrome resistors)
  155-0274-00 (14 pin DIP)

SCHEMATIC



6

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	NOTES	VALUES	UNITS
$V_{out\text{-}sub}$ MAX	Maximum voltage of the outputs (pads 5, 6, 8, 9) relative to the substrate (pad 4).	Prevents collector-substrate breakdown of Q5, Q6, Q7, Q8.	19	V
$V_{out\text{-}cont}$ MAX	Maximum voltage of the outputs (pads 5, 6, 8, 9) relative to the control inputs (pads 11, 12).	Prevents collector base breakdown of Q5, Q6, Q7, Q8.	7	V
$V_{cont\text{-}input}$ MAX	Maximum voltage at the control inputs (pads 11, 12) relative to the inputs (pads 1, 13, 14, 16).	Prevents collector base breakdown of Q1 and Q2.	8	V
$V_{sub\text{-}input}$ MAX	Maximum voltage of the substrate (pad 4) relative to the inputs (pads 1, 13, 14, 16).	Substrate voltage must be held more negative than any collector in the circuit.	0	V
V_{RQ3} MAX	Maximum voltage from pad 7 to pad 11 or 12.	Maximum steering diode reverse voltage to avoid degradation.	2	V
$V_{R11\text{-}12}$ MAX	Maximum voltage from pad 11 to 12 or from pad 12 to pad 11.	Maximum steering diode reverse voltage to avoid degradation.	2.5	V
V_{EB} MAX	Maximum voltage from pad 2 to pads 13 or 16; or from pad 3 to pads 1 or 14.	Maximum base-emitter reverse voltage to avoid degradation.	2	V
I MAX	Maximum current, pads 2 and 3.	Sum of pad 2 current and pad 3 current.	20[a]	mA
Tj MAX	Maximum junction temperature.		125	°C

[a]Contact Applications Engineering, IC Manufacturing if 20 mA/pad is to be exceeded.

PAD IDENTIFICATION

Pad No.	Function	Pad No.	Function
1	INPUT (Q2 Base)	10	NO PAD 10
2	BIAS (Current Source—Q1 Emitter)	11	GAIN ADJUST
3	BIAS (Current Source—Q2 Emitter)	12	GAIN ADJUST
4	SUBSTRATE	13	INPUT (Q1 Base)
5	OUTPUT (Q8 Collector)	14	INPUT (Q2 Base)
6	OUTPUT (Q6 Collector)	15	NO PAD 15
7	GAIN ADJUST Diodes	16	INPUT (Q1 Base)
8	OUTPUT (Q7 Collector)	17	Q1 COLLECTOR
9	OUTPUT (Q5 Collector)	18	Q2 COLLECTOR

ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	MIN	MAX	UNITS
BV_{CEO} Q1, Q2, at 200 μA	4.4		V
BV_{CEO} Q5, Q6, Q7, Q8 at 200 μA	4.4		V
$BV_{CEO\ SUS}$ Q1, Q2 at 10 mA	4.9		V
$BV_{CEO\ SUS}$ Q5, Q6, Q7, Q8 at 10 mA	4.9		V
INPUT BIAS CURRENT Q1 or Q2 (16 mA emitter current)	64	225	μA
NORMAL OFFSET	−14	+14	mV
INVERT OFFSET	−14	+14	mV
NORMAL GAIN	2.68	2.96	
INVERT GAIN	2.68	2.96	
NORMAL-INVERT GAIN MATCH	−0.5	+0.5	%
NULL OFFSET	−10	+10	mV
NULL GAIN	−.14	+.14	
50% GAIN	.49	.51	$X(AV_{NORM})$
OFF FEEDTHRU	−200	+200	μV

PARAMETRIC DEFINITIONS

The 203-0084-90 is specified in three different operating conditions: NORMAL, INVERT, and NULL.

In the NORMAL condition, Q5 and Q8 are conducting and Q6 and Q7 are not.

In the INVERT condition, Q6 and Q7 are conducting and Q5 and Q8 are not.

In the NULL condition, Q5, Q6, Q7 and Q8 are all conducting equally.

APPLICATIONS INFORMATION

Output Stage Considerations

Pads 7 and 12 can be voltage driven and pad 11 left open (Figure 1) if gain linearity as a function of control voltage is not critical. The voltage applied on pads 7 or 12 should be 1.2 to 3.7 volts above the quiescent voltage on pads 1, 14, 13, 16 for conducting output transistors. For nonconducting output transistors pad 7 or 12 can be at a lower potential than this. Absolute maximum ratings must be observed however. For the case of pad 7 and 12 voltage driven and pad 11 open, gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{\exp\left(\frac{qV_{14}}{kT}\right) - \exp\left(\frac{qV_7}{kT}\right)}{\exp\left(\frac{qV_{14}}{kT}\right) + \exp\left(\frac{qV_7}{kT}\right)}\right]$$

where $A_{V\,NORM}$ = Normal Gain

V_7 = voltage applied on pin 7
V_{14} = voltage applied on pin 12
$\frac{kT}{q}$ = 26 mV at room temperature

If gain linearity as a function of control voltage is critical, pins 7 and 12 should be current driven and pin 11 returned to a voltage so as to set pins 7 and 14 voltage to the proper level as mentioned above. Figure 2 shows this type hookup. Current driving these inputs linearizes the gain by making use of the exponential current-voltage relationship of the diodes Q3 and Q4 to cancel that of the output transistors. The gain is given by:

$$A_V = A_{V\,NORM}\left[\frac{I_{14} - I_7}{I_{14} + I_7}\right]$$

where I_7 = current into pin 7
I_{14} = current into pin 12

If variable gain of only a single polarity is desired, one pair of outputs can be used and the other pair connected to separate unused loads as in Figure 3.

If fixed maximum gain is desired, one pair of outputs can be left open as in Figure 4.

In applications where the output is to be switched from one output pair to another, the difference in offset voltage between the two outputs should not be specified any tighter than 28 mV (the sum of normal and invert offset specifications).

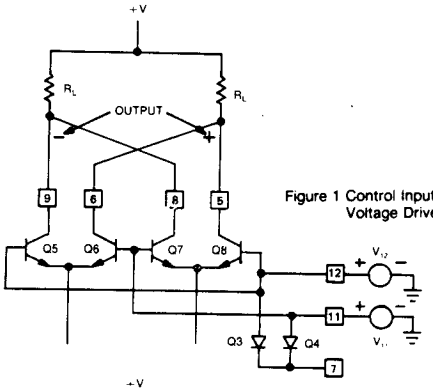


Figure 1 Control Inputs Voltage Driven

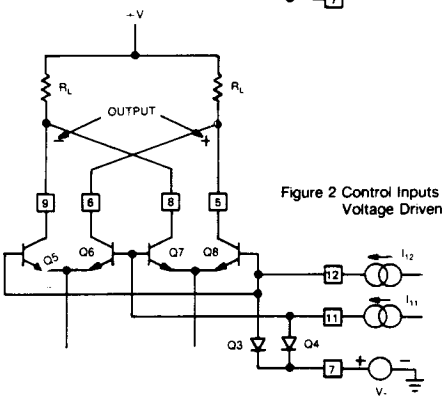
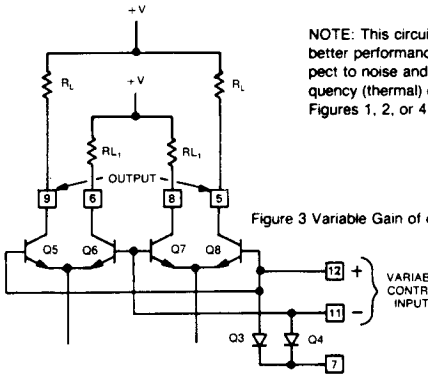
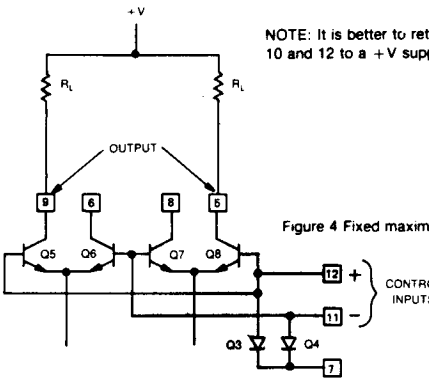


Figure 2 Control Inputs Voltage Driven



NOTE: This circuit provides better performance with respect to noise and low frequency (thermal) errors than Figures 1, 2, or 4.

Figure 3 Variable Gain of one polarity only



NOTE: It is better to return 10 and 12 to a +V supply if possible.

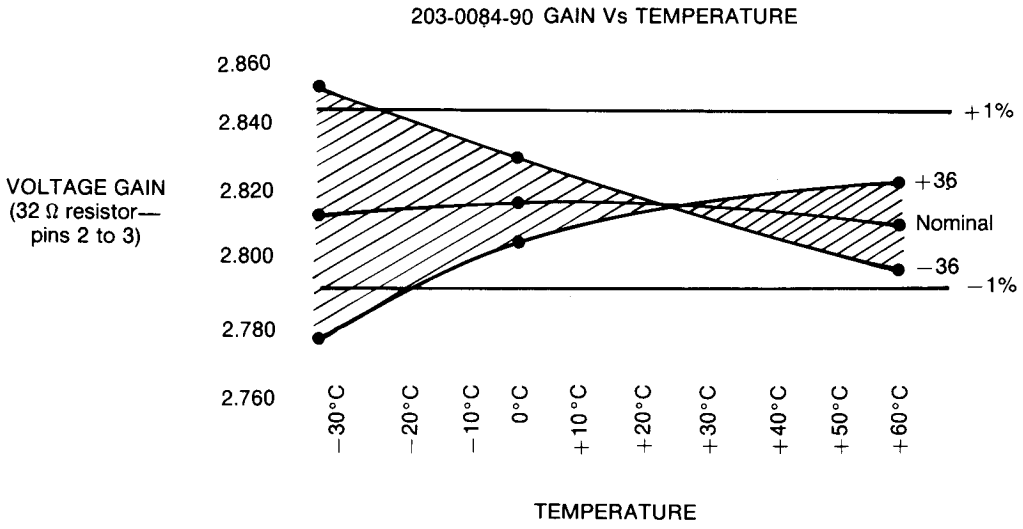
Figure 4 Fixed maximum gain

APPLICATIONS INFORMATION (cont)

Input Stage Considerations

The bias current (pin 2 and 3 current) should not exceed 18 mA per side or a decrease in the life of the part may result.

Typical Performance Graph
(not a specification, for information only)



PRODUCT PRECAUTIONS

Input Protection

Input base-emitter voltages should not exceed 2 V in the negative direction and 1 V in the positive direction.

Output Loading

Outputs should be limited to less than those listed in Absolute Maximum Ratings.

Power Supply Turn-On/Turn-Off Sequence

Substrate voltage should be turned on coincident with or before the other voltages.

Handling Procedures

Static sensitive handling procedures should be implemented for this part.

6

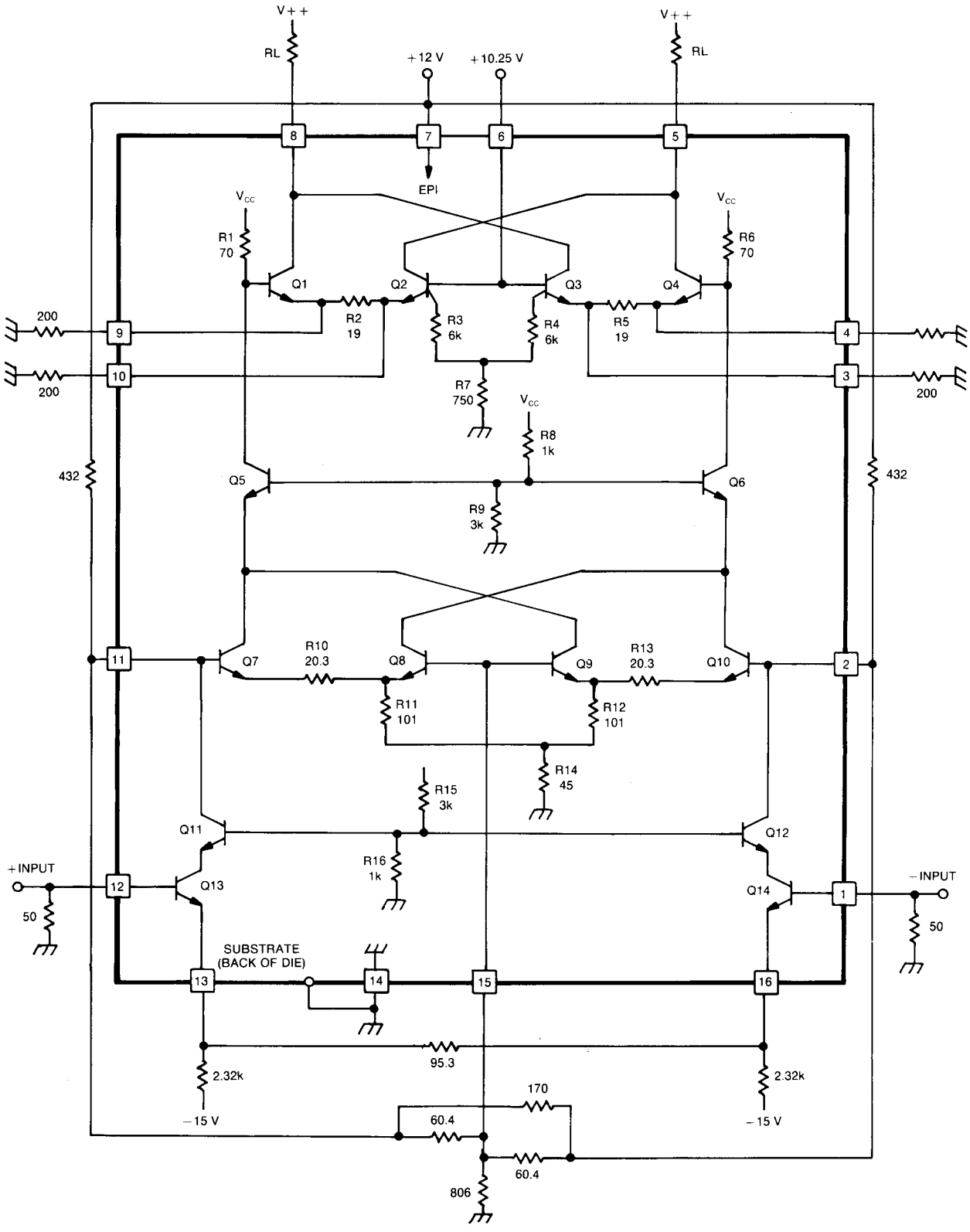
VERTICAL OUTPUT DIE

DESCRIPTION

The 203-0089-91 is a high frequency, 3 stage current gain amplifier. The circuit has differential inputs and outputs and is designed to be driven from a balanced 50 Ω source. It is capable of supplying large output current swings.

FEATURES

- 3 stage current gain amplifier
- Ft doublers
- 600 MHz bandwidth
- 160 mA output current


V++
RL
+12 V
+10.25 V
V++
RL
8
7
6
5
EPI
V_{CC}
V_{CC}
R1
70
R6
70
Q1
Q2
Q3
Q4
200
R2
19
R3
6k
R4
6k
R5
19
9
4
10
3
200
200
R7
750
V_{CC}
R8
1k
432
Q5
Q6
432
R9
3k
11
Q7
R10
20.3
Q8
Q9
R13
20.3
Q10
2
R11
101
R12
101
R14
45
R15
3k
Q11
Q12
+INPUT
12
Q13
R16
1k
Q14
1
−INPUT
50
50
SUBSTRATE
(BACK OF DIE)
13
14
15
16
95.3
2.32k
2.32k
170
−15 V
60.4
−15 V
60.4
806

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATIONS	NOTES	VALUES	UNITS
$V_{3,4,9,\&10}$ MAX	Maximum voltage to be applied from pad 3, 4, 9 & 10 to pad 14 (ground).		12.5	V
$V_{5,8\text{-}Sub}$ MAX	Maximum voltage allowable from pad 5 to substrate or from pad 8 to substrate.	Substrate is back of die.	15.5	V
$V_{5\text{-}4,10}$ MAX	Maximum voltage allowable from pad 5 to pad 4 or 10.	Maximum C-E voltage of output transistors Q2 & Q4.	4.0	V
$V_{8\text{-}3,9}$ MAX	Maximum voltage allowable from pad 8 to pad 3 or 9.	Maximum C-E voltage of output transistors Q1 & Q3.	4.0	V
$V_{12\text{-}13}$ $_{16\text{-}1}$ MAX	Maximum voltage allowable on pad 13 with respect to pad 2 or on pad 16 with respect to pad 1.	Maximum reverse bias on B-E junction of Q13 & Q14.	2.0	V
I_{OUT} MAX	Maixmum output current pad 5 or pad 8.		160	mA
T_J	Operating junction temperature		−15 to +125	°C
T_{STG}	Storage temperature		−55 to +125	°C

Maximum Assembly Temperature

Die Attach	1 Minute Maximum	400	°C
Die Attach Adhesive Cure	2 Hours Maximum	150	°C
Wire Bond	1 Minute Maximum	350	°C
Bake Out/Lid Attach	2 Hours Maximum	175	°C

6

PAD IDENTIFICATION

Pad #	Description
1	− signal input
2	1st stage collector supply
3, 4	3rd stage emitter current source
5	+ signal output
6	3rd stage bias
7	V_{CC}
8	− signal output
9, 10	3rd stage emitter current source
11	1st stage collector supply
12	+ signal input
13	1st stage emitter current source
14	substrate gnd
15	2nd stage bias
16	1st stage emitter current source

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
I_{OS}	Output Offset Current ($I_5 - I_8$) Input Current = 0	−8.2	8.2	mA
Ai_0	Current Gain (Ctr. Screen) Input Current = 0 + Δ See Note 1	13.85	20.65	
Ai_1	Current Gain (Top Screen) Input Current = 1.5 mA + Δ See Note 1	13.85	20.65	
Ai_2	Current Gain (Bot. Screen) Input Current = 1.5 mA + Δ See Note 1	13.85	20.65	
Ai_1	Gain Linearity	−5.0	+5.0	%
Ai_2	Gain Linearity	−5.0	+5.0	%
	f_T of test key transistor at V_{CE} = 4 V, I_C = 80 mA	1.5	4	GHz

NOTE 1: As tested in the Test Circuit.

DEFINITIONS

Output Offset Current, IOS

The difference in current flowing in the two outputs with zero input current.

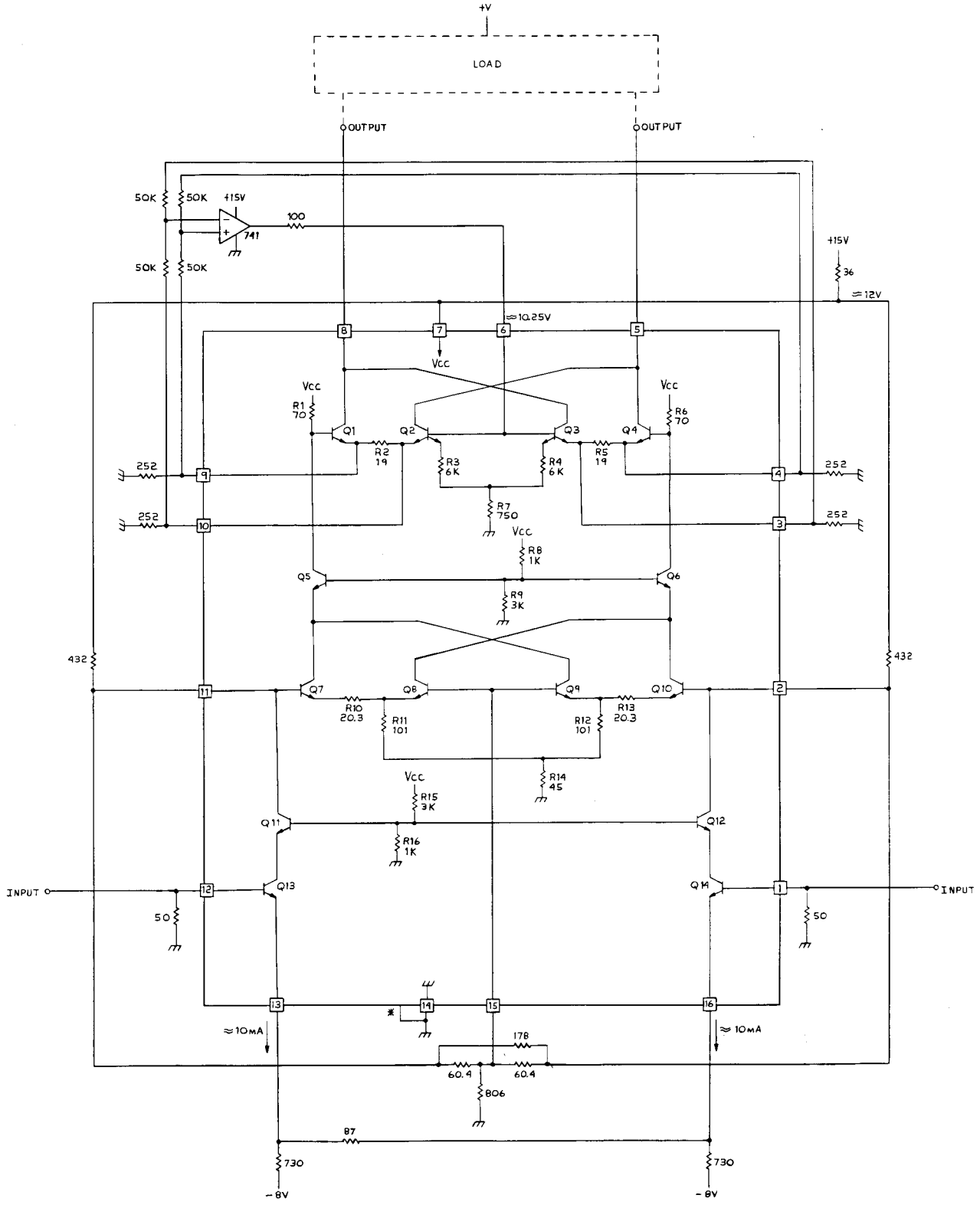
Current Gain, Ai

For determining current gain the die is assumed to be differentially driven by a current source. Current flowing into one input flows out the other input ($I_B = I_A$ in Figure 2). The current "loops" through the amplifier and is known as "Input Loop Current".

Three gains are specified, with different quiescent input currents:

	Gain	Quiescent Input Loop Current	Change in Input Loop Current (Δ)
(Center Screen)	Ai_0	0	+1.0 mA to −1.0 mA Change (2 mA pk to pk signal)
(Top Screen)	Ai_1	1.5 mA	+1.0 mA to −1.0 mA Change (2 mA pk to pk signal)
(Bottom Screen)	Ai_2	−1.5 mA	+1.0 mA to −1.0 mA Change (2 mA pk to pk signal)

All parameters are specified per the schematic diagram and are valid only at 25°C ambient temperature. This circuit approximates the usage in the 155-0077-00 part number as used in the 7704A instrument. The load is assumed to provide current paths from a positive supply to the outputs. The op-amp automatically balances the circuit. This could alternately be done manually by varying the voltage at pad 10 for maximum gain. The 50 Ω resistors on the inputs are considered to be an integral part of the amplifier. That is, the inputs are defined to be the points indicated as "input" in Figure 1.



NOTE:
1. * SUBSTRATE ON BACK OF DIE.

FIGURE 1

APPLICATION TO DRIVE CRT DEFLECTION PLATES

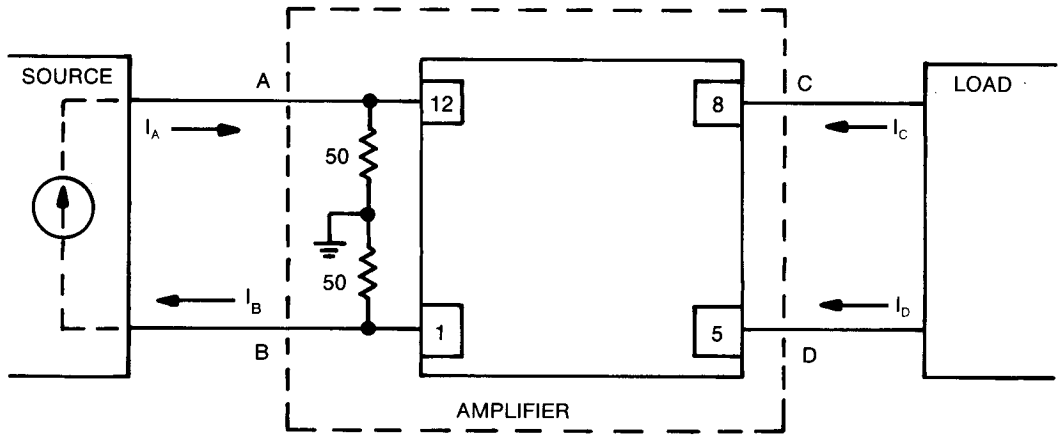


FIGURE 2

DEFINITIONS (continued)

Currents I_C and I_D of Figure 2 always flow into the die as they are collector currents of transistors. With no signal applied to the input, the output currents should be equal except for offset currents. With input applied, the output currents swing above and below their quiescent value with one current change, ΔI_C or ΔI_D ($\Delta I_C = \Delta I_D$ nominally), appears to flow in a loop into one output and out the other. The term "Output Loop Current" is used to describe variations in the output currents from quiescent conditions.

Current gain is defined as:

$$Ai_0 = \frac{\Delta I_C - \Delta I_D}{\Delta I_A + \Delta I_B}$$

Gain Linearity

Sometimes called gain compression or expansion. This parameter measures the change in small signal gain as a function of input quiescent current, expressed as a percent.

$$\Delta Ai_1 = \frac{Ai_1 - Ai_0}{Ai_0} \times 100\%$$

$$\Delta Ai_2 = \frac{Ai_2 - Ai_0}{Ai_0} \times 100\%$$

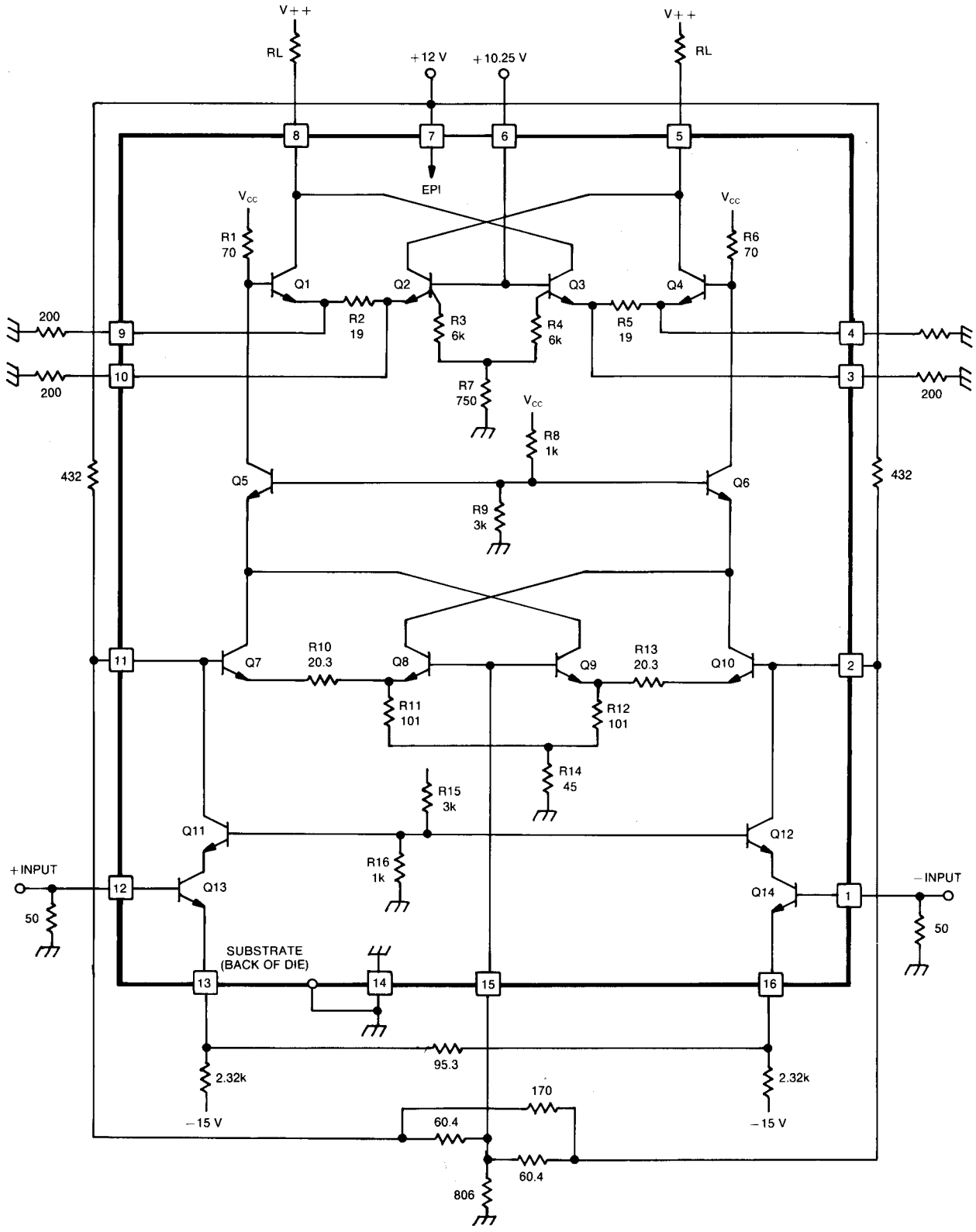
APPLICATIONS INFORMATION

Typical Bias Configuration

Figure 3 shows a typical biasing scheme for the device.

Electrical Considerations

Typical DC operating voltages and currents are indicated in Figure 3.



NOTE: The circuit was designed for optimum performance at these bias voltages. Caution should be exercised in making significant changes from these levels.

FIGURE 3

APPLICATIONS INFORMATION (cont)

Biasing

In general, the biasing is accomplished as follows:

1. Apply 12 volts to pad 11 and approximately 10.25 volts to pad 10.
2. Decide on the standing output current on pads 9 and 12. This current should not exceed 80 mA per side. Choose the resistors on pads 7, 8, 14, 15 to provide half of this current at each emitter (not to exceed 40 mA). The voltage at these points is about one V_{BE} drop below the pad 10 voltage or about 9.5 volts.
3. The currents flowing out of the emitters from pads 2 and 4 through resistors to the negative supplies are chosen. These currents are referred to as the "tail" currents.
4. Apply approximately 5.75 volts to pad 3.
5. Choose the biasing networks on pads 6 and 16 to provide a voltage of approximately 6 volts. This voltage must be approximately .25 volt higher than that applied at pad 3 to provide equal currents in Q1 and Q8 and in Q9 and Q10. The current flowing into pads 6 and 16 is approximately the pad 2 and 4 tail current multiplied by .98 (Q13, Q14 x Q11, Q12 $\simeq$ .98).

NOTE: The circuit was designed for optimum performance at these bias voltages. Caution should be exercised in making significant changes from these levels.

Gain Polarity

The gain polarity is as follows:

An increase in current into pad 1, or a decrease in current into pad 5, causes the current flowing into pad 12 to increase and the current flowing into pad 9 to decrease.

APPLICATIONS INFORMATION (cont)

Typical Load Configuration

The typical application is in a hybrid used to drive the vertical deflection plates of a CRT. Two discrete output transistor chips are included in the hybrid to provide the large voltage swings necessary.

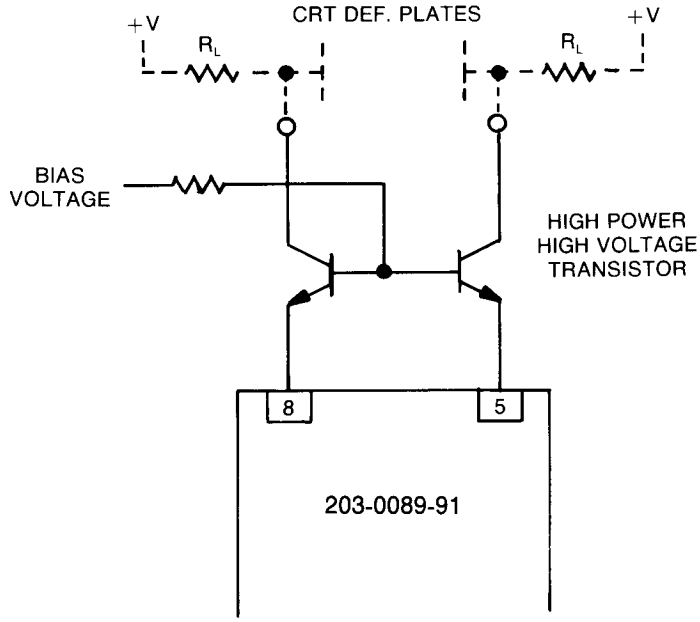


FIGURE 4
APPLICATION TO DRIVE CRT DEFLECTION PLATES

It should be noted, that although this die is capable of delivering up to 80 mA per side, application of these capabilities becomes dependent on the output discrete transistors packaged in the hybrid(s). Device history shows that vertical output applications of 100 MHz BW driving a small screen (portable) oscilloscope are not drive limited. However, large screen and/or 250 MHz BW instruments do not always make gain/aberration (bandwidth requirements with acceptable plant yields).

The minimum gain has been adjusted so that the die plus discrete output transistors with Beta $\geqslant$30 will pass the hybrid spec of 13.85 to 20.65.

4-BIT PARALLEL A/D CONVERTER

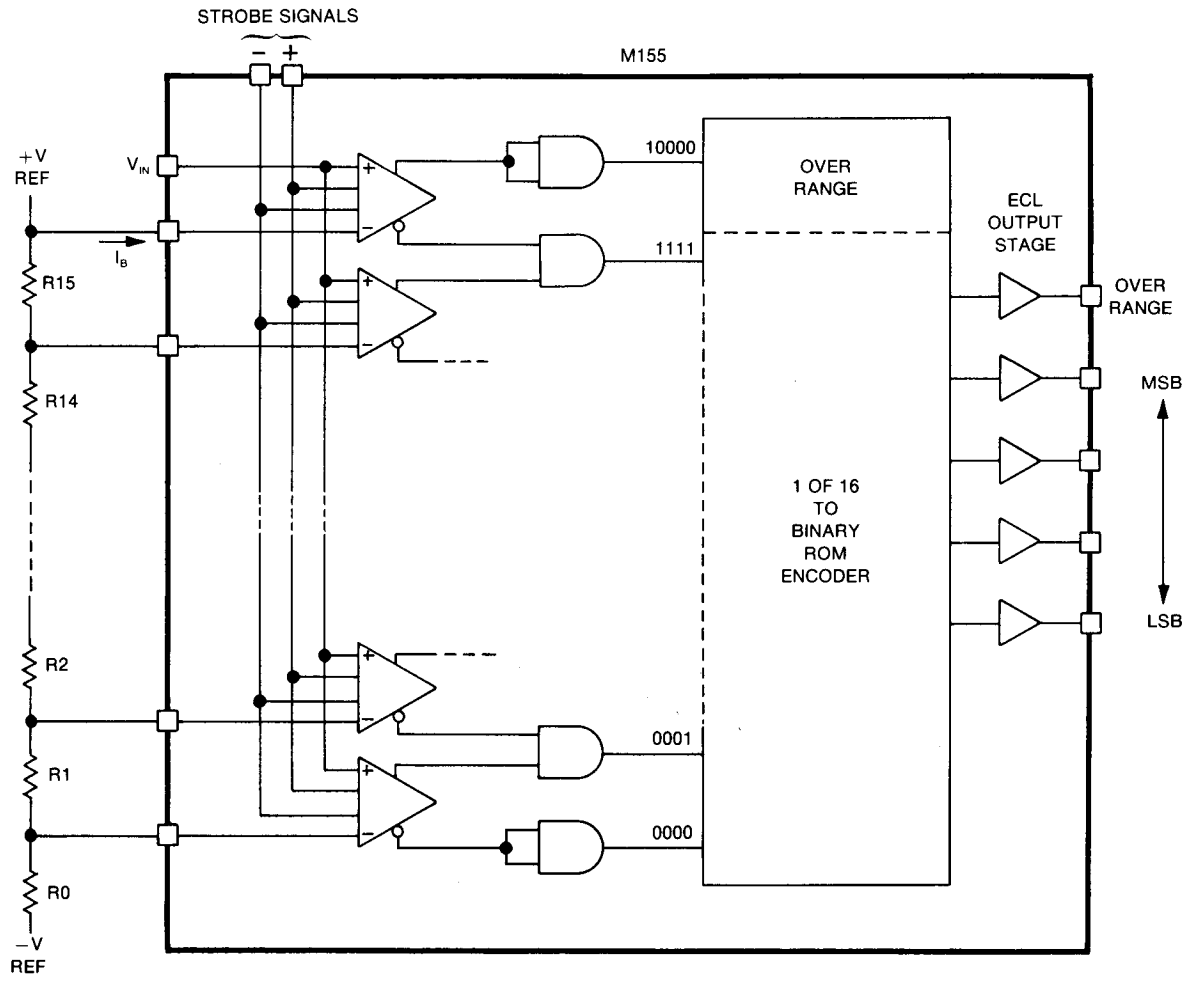
DESCRIPTION

The 203-0155-91 is a 17 level digitizer, designed for use in parallel-series A/D converter systems. It consists of 16 comparator cells, digital encoding, circuitry, and output drivers.

FEATURES

- 80 MHz Maximum Clock Rate
- 850 mW Power Dissipation
- ECL Output
- Two 203-0155-01's may be combined for a 5-bit parallel A/D converter
- 5 MHz Input Bandwidth

BLOCK DIAGRAM



6

ABSOLUTE MAXIMUMS

Symbol	Limits	Units	Notes
V_{CC}	0 to +6	V	
V_{BB}	0 to +6	V	
V_{EELIN}	−6 to 0	V	
V_{EEDIG}	−6 to 0	V	
$V_{CC} - V_{BB}$	0 to 6	V	
V_{IN}	−1.65 to 3.2	V	
Vi, i = 1-16	−1.65 to 3.2	V	
V_{IN} − Vi, 1 = 1-16	0 to 3.3	V	See Note
I (ECL OUT)	0 to 10	mA	Output Current From B_0, B_1, B_2, B_3, B_X
V_{SP}	−2 to −4	V	
V_{SN}	−2 to −4	V	

NOTE: Maximum differential voltage between V_{IN} and any Vi (i = 1-16) should not exceed 3.3 V. Larger voltages may degrade the current gain of input transistors which will affect offset voltage. This results from reverse bias of emitter-base diodes.

MAXIMUM STORAGE TEMPERATURES

Non-Destructive (In Clean, Dry Environment) 75°C

OPERATING JUNCTION TEMPERATURES

a. Accelerated Burn In After Assembly Into Hybrid 125°C

b. In Product Service 125°C

Assembly

Die Attach	1 Minute Maximum	400°C
Wire Bond	1 Minute Maximum	350°C
Bake Out/Lid Attach	2 Hours Maximum	175°C

TERMINAL IDENTIFICATION

Pad No.	Name	Input/Output	Description
1	V_{SN}	Input	Negative Strobe
2	V_{SP}	Input	Positive Strobe
3	V_{EELIN}	Supply	Negative Analog Supply
4	V_1	Input	Reference Voltage (Lowest)
5	V_2	Input	Reference Voltage
6	V_3	Input	Reference Voltage
7	V_4	Input	Reference Voltage
8	V_5	Input	Reference Voltage
9	V_6	Input	Reference Voltage
10	V_7	Input	Reference Voltage
11	V_8	Input	Reference Voltage
12	V_9	Input	Reference Voltage
13	V_{10}	Input	Reference Voltage
14	V_{11}	Input	Reference Voltage
15	V_{12}	Input	Reference Voltage
16	V_{13}	Input	Reference Voltage
17	V_{14}	Input	Reference Voltage
18	V_{15}	Input	Reference Voltage
19	V_{16}	Input	Reference Voltage (Highest)
20	V_{IN}	Input	Analog Input
21	GND-LIN	Supply	Analog Ground
22	V_{CC}	Supply	Positive Supply
23	GND-DIG	Supply	Digital Ground
24	B_3	Output	MSB
25	B_X	Output	Over-Range
26	B_0	Output	LSB
27	B_1	Output	LSB +1
28	B_2	Output	LSB +2
29	V_{EE}-DIG	Supply	Negative Digital Supply
30	V_{BB}	Supply	Base Bias Supply

ELECTRICAL CHARACTERISTICS

Parameter/Conditions	Symbol	Min	Max	Units
Positive Supply (5.0 V)	V_{CC}	4.8	5.5	V
Base Supply (3.7 V)	V_{BB}	$V_{IN}+0.7$	3.7	V
Negative LIN Supply (−5.2 V)	V_{EE}-LIN	−5.5	−5.0	V
Negative DIG Supply (−5.2 V)	V_{EE}-DIG	−5.5	−5.0	V
Positive Supply Current (Nominal Supply Voltages)	$I(V_{CC})$	60	100	mA
Base Supply Current (Nominal Supply Voltages)	$I(V_{BB})$	0.1	0.8	mA
Negative LIN Supply Current (Nominal Supply Voltages)	$I(V_{EELIN})$	28	52	mA
Negative DIGITAL Supply Current (Nominal Supply Voltages)	I_C $I(V_{EE}$-DIG)	23	45	mA
Input Range	V_{IN}	−1.536	+1.536	V
Reference Input Range	Vi i = 116	−1.536	+1.536	V
Differential Input Range	V_{IN}-Vi	−3.2	3.2	V
Strobe Levels	V_{SP} V_{SN}	−3.35	−3.15	V
Analog Input Bias Current	$I(V_{IN})$	15	160	μA
Reference Input Current	$I(V_{IN})$ i = 116	1.0	10	μA
ECL-OUT Low	$V_{OUT}(LO)$	−2.0	−1.6	V
ECL-OUT High	$V_{OUT}(HI)$	−0.98	−0.7	V
Differential Offset Non-Linearity Guaranteed over V_{IN} Range	ΔV_{OS}	−5 −1.5	+5 +1.5	mV V

f_T of test key transistors: 1.8 GHz min. at V_{CE} = 4 V, I_C = 2 mA.

Applications Information

To function properly, it is required that the reference voltage inputs be monotonically increasing from V_1 to V_{16}. The binary output code "rolls over" from 01111 to 10000 when V_{IN} is greater than V_{16}.

Two chips may be connected together to form a 5-bit parallel A/D converter. The referenece voltage inputs are stacked in series while the analog input and strobe lines are connected in parallel. The four lower order bits may be wired together by pairs with the over range bit of the lower chip becoming the MSB.

Careful attention to layout is essential as the part is susceptible to interaction of the strobe signals and input and references. A small (22 Ω) resistor in the input line is helpful. Bypassing close to the circuit is needed.

V_{BB} should not come up before V_{CC}.

6

ECL D/A DIE

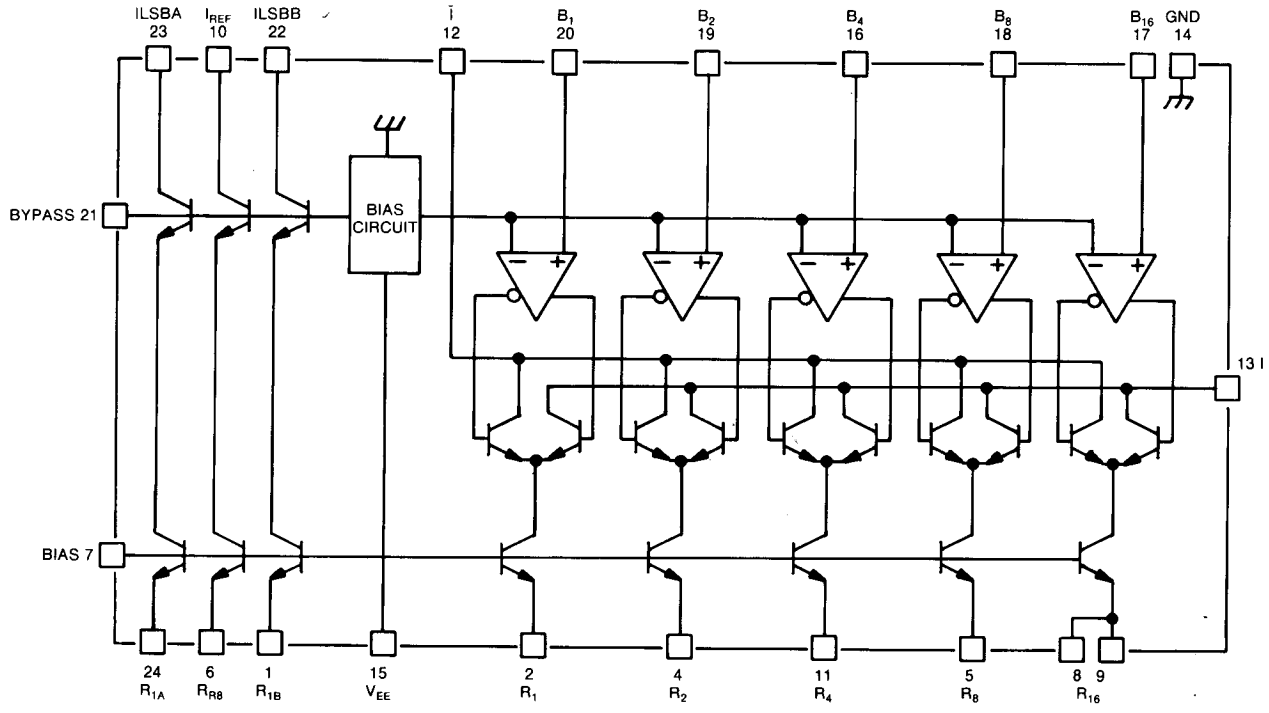
DESCRIPTION

The 203-0177-90 is designed for use with the 203-0155-00 in parallel serial A/D converter systems. Five precision binary scaled current sources are independently switched to either I or $\bar{I}$, two supplementary current outputs. Switching is done by an emitter coupled pair driven differentially by an amplifier which converts the single ended input to a level-shifted differential drive.

FEATURES

- 5 BIT DAC
- Settling time to 8 bits 20 ns (240 Ω, 10 pF load)
- Power Supply −5.2 volts
- Input ECL compatible
- Two unswitched LSB current sources

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

ELECTRICAL SYMBOL	VALUE	UNITS
B_1	−4 to 0	V
B_2	−4 to 0	V
B_4	−4 to 0	V
B_8	−4 to 0	V
B_{16}	−4 to 0	V
Bias	−12 to −2	V
I	−2 to +5	V
$\bar{I}$	−2 to +5	V
I_{1A}	−2 to +5	V
I_{1B}	−2 to +5	V
F_B	−2 to +5	V
V_{EE}	−6 to 0	V

Emitter connections R_1, R_{1A}, R_{1B}, R_2, R_4, R_8, R_{R8}, and R_{16} should never be more positive than Bias.

Bypass must not be pulled down externally below −1.5 volts.

TERMINAL IDENTIFICATION

PIN NUMBER	NAME	INPUT/OUTPUT	DESCRIPTION
1	R_{1B}	Current Source	ILSB A Current
2	R_1	Current Source	ILSB A Current
4	R_2	Current Source	2ILSB Current
5	R_8	Current Source	8ILSB Current
6	R_{R8}	Current Source	Emitter Reference Current
7	BIAS	Output	
8,9	R_{16}	Current Source	16 ILSB (MSB) Current
10	IREF	Input	Collector Reference Current
11	R_4	Current Source	4ILSB Current
12	$\bar{I}$	Output	Supplementary Current Output
13	I	Output	Current Output
14	GND		Ground
15	VEE	Neg. Supply	
16	B_4	Input	LSB +2 Input
17	B_{16}	Input	MSB Input
18	B_8	Input	LSB +3 Input
19	B_2	Input	LSB +1 Input
20	B_1	Input	LSB Input
21	Bypass	Output	Bypass Capacitor
22	ILSB B	Output	Utility LSB Current Output-B
23	ILSB A	Output	Utility LSB Current Output-A
24	R_{1A}	Current Source	ILSB B Current

ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITIONS	SYMBOL	MIN	MAX	UNITS
Logical "Low" to Inputs B_1, B_2, B_4, B_8, B_{16},	ECL (Lo)	−2.0	−1.62	V
Logical "High" to Inputs B_1, B_2, B_4, B_8, B_{16},	ECL (Hi)	−0.96	−0.7	V
Negative Supply	V_{EE}	−5.5	−5.0	V
Nominal = 6.4 mA Reference Current	I_{REF}		8	mA
Nominal = 12.8 mA Most Significant Bit Current	I_{MSB}		16	mA
Output Compliance	I $\bar{I}$	−1.6	3.5	V
Output Compliance	I_{1A} I_{1B}	−1.6	3.5	V
Bias for Current Sources	Bias	−9	−2.7	V
Power Supply Current V_{EE} (Dig)	$I\ (V_{EE}-D)$	−15	−10	mA
Non-Linearity (Full Scale)*	Error		0.025	% Error
Non-Linearity (Full Scale)*	Error		0.1	% Error

***Non-linearity is defined to be sure of absolute values and therefore must be non-negative.**

6

APPLICATIONS INFORMATION

The part is designed to operate with a reference of +3.072 volts or ±1.536 volts. Full scale output current is then 25.6 mA. A −5.2 volt digital supply is needed to set up the reference current. Digital inputs are ECL compatible and sink 1 mA each.

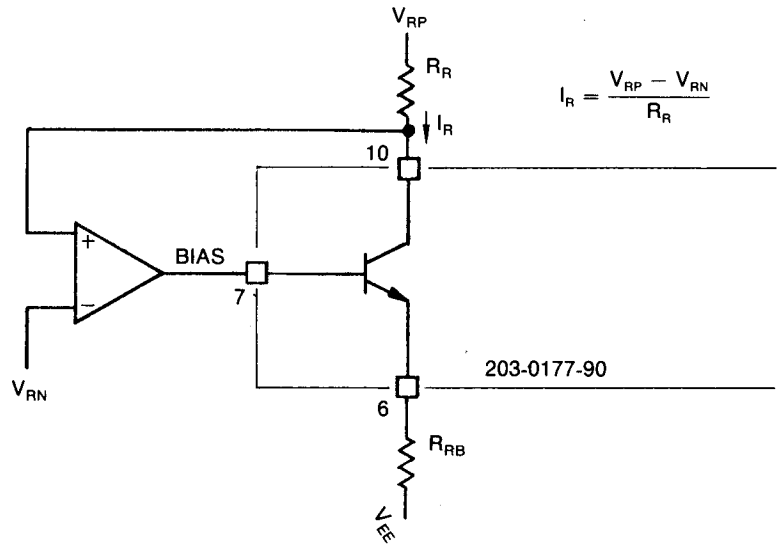
The component is tested to have linearity better than ±0.05% (±1/2 LSB at 10 bits). More specifically, the 4 LSB currents ratio binarily to the MSB current within ±0.05% of full scale where full scale is defined to be twice the MSB current. Differential non-linearity is also tested so that each 1-bit transition causes an output change of 1/32 of full scale ±0.05% full scale. A final check of overall linearity is made by testing that the sum of the absolute values of each bit current error is less than 0.1% of full scale. This guarantees an overall non-linearity of less than ±0.05%.

Because of the finite and variable output resistance, maximum accuracy will be achieved by operating the output into a fixed voltage. It is expected that this will be necessary to achieve 10-bit accuracy.

Greatest accuracy may be attained by functional trimming the emitter current setting hybrid resistors. The trimming should be done with output voltage constant.

To minimize the effect of emitter-base diode offsets and drifts a large voltage should be maintained across the emitter current setting resistors. At least 1 V for 8-bit accuracy and 4 V for 10-bit.

In connecting the biasing feedback loop, it should be observed that there is an inverting gain within the IC and the op-amp inputs must be as indicated in the figure below.



BIASING CIRCUIT FOR 203-0177-90

Pin 21 (bypass) is a voltage supply derived on the IC (about −1.9 V). Slightly faster settling of the output may be realized by bypassing this node with a capacitor (about 0.1 μF) to ground.

Digital input signals should not exceed the ECL range, −0.7 V to −2.0 V during operation to avoid saturating transistors within the IC.

The utility current sources ILSBA and ILSBB are designed to carry one LSB current and are provided for a specific application. They may be used as required. If unused, it is recommended that the emitters be connected to Bias (Pin 7) and the collectors to Bypass (Pin 21).

6

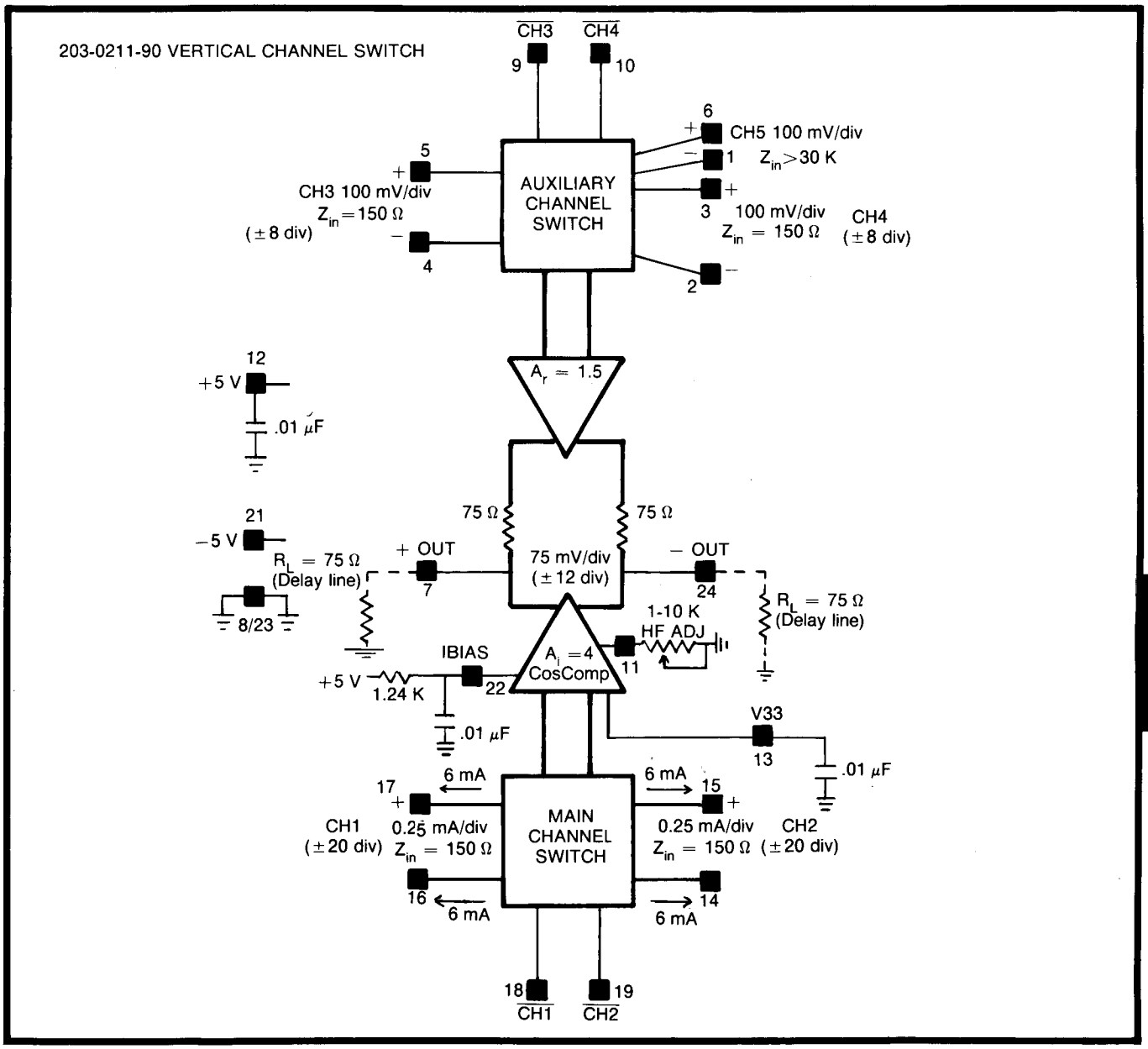
CHANNEL SWITCH DIE

DESCRIPTION

The 203-0211-90 is a four input one output channel switch and amplifier intended for 300 MHz vertical deflection systems. Four TTL compatible control pins allow selection of any one of the four inputs or the sum of CH1 and CH2.

FEATURES

- 600 MHz bandwidth
- Output intended to drive 150 Ω load
- CH1 & CH2
  - Current driven
  - Differential transresistance (75 mV per Div/.25 mA per Div) is 300 Ω ±3%
- CH 3, 4, & 5
  - Voltage driven
  - Voltage gain .75 ±2%



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	MIN	MAX	UNITS
T_J	Operating Junction Temperature	−15	+125	C
T_{STG}	Storage Temperature	−62	+125	C
V-VS	Maximum Input Voltage −VS1, −VS2, −VS3, −VS4 Maximum Input Range	−.3	VCC5 + .3	V
	CH1 & CH2 Differential Inputs	−2.0	+5.0	V
	CH3 & CH4 & CH5 Maximum Input range	−1.5	+1.5	V
I-CH1] ICH2	Maximum Input Current Range CH1 & CH2 Differential Inputs	+.01	−24	mA
V-CC5	+5 V Supply	−0.3	7.0	V
V-EE5	−5 V Supply	+0.3	−7.0	V
V-HFADJ	HFADJ Voltage	−5.0	+5.0	V
V-IBIAS	IBIAS Voltage	−5.0	+5.0	V

Assembly

Die Attach	1 minute maximum	400°C
Wire Bond	1 minute maximum	350°C
Bake Out/Lid Attach	2 hours maximum	175°C

6

TERMINAL IDENTIFICATION

PAD #	NAME	INPUT/OUTPUT	DESCRIPTION
1	CH5−	Input	CH5 Inverting Input
2	CH4−	Input	CH4 Inverting Input
3	CH4+	Input	CH4 Noninverting Input
4	CH3−	Input	CH3 Inverting Input
5	CH3+	Input	CH3 Noninverting Input
6	CH5+	Input	CH5 Noninverting Input
7	+Out	Output	+ Differential Output
8	Gnd		Ground Terminal
9	CH3/Not	Input	CH3 Select
10	CH4/Not	Input	CH4 Select
11	HFADJ	Bias	High Frequency Adjust
12	VCC5	Bias	+5 V Supply
13	Bypass		Bypass (.01 μF to GND)
14	CH2−	Input	CH2 Inverting Input
15	CH2+	Input	CH2 Noninverting Input
16	CH1−	Input	CH1 Inverting Input
17	CH1+	Input	CH1 Noninverting Input
18	CH1/Not	Input	CH1 Select
19	CH2/Not	Input	CH2 Select
20	V31	Test	Test Point
21	VEE5	Bias	−5 V Supply
22	IBIAS	Bias	Bias Input
23	GND		Ground Terminal
24	−Out	Output	− Differential Output

ELECTRICAL CHARACTERISTICS

NUMBER	CONDITIONS	MIN	MAX	UNITS
1	DC Channel Isolation	300:1		
2	CH1, CH2 Differential Transresistance mV Output/mA Input 75 mV per div/.25 mA per div	292.5	307.5	Ω
3	CH1 & CH2 Small Signal Gain w/300 mV output. (% of center screen gain)	98.2	99.5	%
4	CH3 & CH4 & CH5 Differential Voltage Gain	.735	.765	
5	CH1 & CH2 Gain Mismatch	−.5	.5	%
6	CH3 & CH4 & CH5 Gain Mismatch Calculated	−.5	.5	%
7	CH1 or CH2 to CH3, CH4, CH5 Mismatch (gain)	−3.0	3.0	%
8	CH1, CH2 add mode, difference from CH1 mode gain	−1.0	1.0	%

ELECTRICAL CHARACTERISTICS (cont)

NUMBER	CONDITIONS	MIN	MAX	UNITS
9	CH1, CH2 Input Common Mode bias voltage at −12 mA common mode bias current	−0.350	−0.500	V
10	CH5 Input Resistance, each side Pad 1 to 8, Pad 6 to 8	15K		Ω
11	CH5 Bias Current at 0 V input Pads 1 & 6	−10.0	100	μA
12	VS1, VS2, VS3, VS4 Bias current at 0.4 V input Bias current at 2.4 V input VIL Valid Range for Low Data VIH Valid Range for High Data	 −0.60 −10.0 −.30 2.0	 +0.0 +10.0 +.80 VCC5 + .3	 mA μA V V
13	CH3, CH4 Common Mode Bias Voltage Inputs Open Pads 2 & 3, 4 & 5	−50	+50	mV
14	Output Common Mode Voltage Pads 7 & 25	−50	+50	mV
15	VEE5 Current Range Pad 23	−90	−140	mA
16	VCC5 Current Range Pad 12	100	140	mA
17	Input Resistance Differential Input CH1 (Pads 17 & 18) CH2 (Pads 15 & 16) CH3 (Pads 4 & 5) CH4 (Pads 2 & 3)	 145 147	 153 153	 Ω Ω
18	Output Resistance Each side of differential output Pads 7 & 24	 73.5	 76.5	 Ω
19	Output Offset for Channels 1, 2, 3, 4	−37.5	+37.5	mV
20	Output Offset for Channel 5	−20.0	+20.0	mV
21	Output Offset, Add (CH1 + CH2) Mode	−75	+75	mV
22	IBIAS, Bias Voltage Range	−0.100	+0.100	V
23	HFADJ, Bias Voltage Range	−3.65	−4.75	V
24	Power Dissipation (For Reference Only)		1.2	W

VERTICAL OUTPUT AMPLIFIER

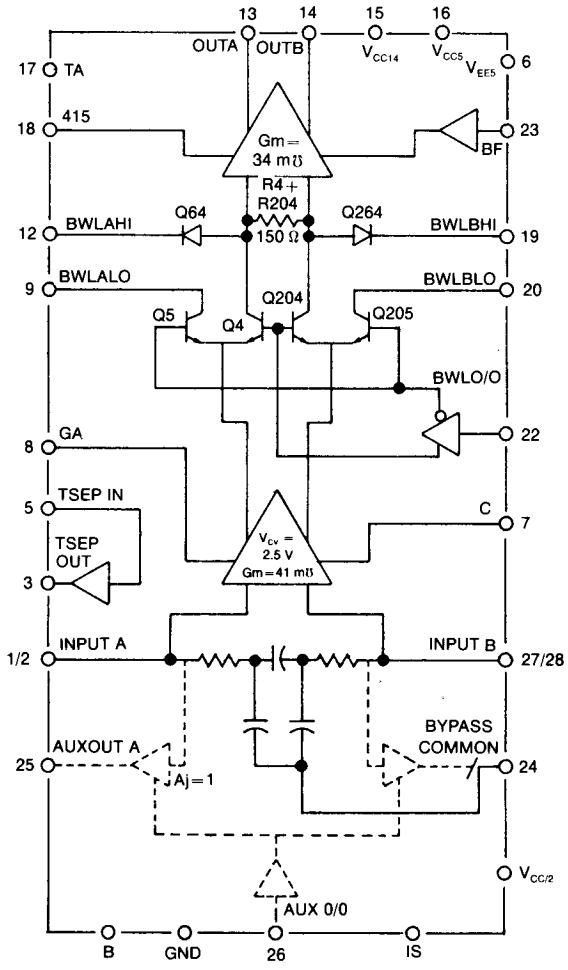
DESCRIPTION

The 203-0212-90 is a high bandwidth, high gain, high linearity, low thermal distortion, vertical output amplifier. The IC is configured as a two stage differential input/differential output transconductance block utilizing the cascomp error correcting topology in each stage. It is intended to drive a common base output stage to provide necessary voltage compliance.

FEATURES

- Potentiometer controlled gain
- Centering adjustments
- Trace separation amp
- Beam find
- TTL compatible gating
- Low power dissipation
- SHIII process
- DC to 660 MHz bandwidth

BLOCK DIAGRAM



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ABSOLUTE MAXIMUMS

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
T_J	Operating Junction Temperature	−15	+150	°C
T_{STG}	Storage Temperature	−55	+150	°C
Pad 1 Pad 2	Input "A"	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 27 Pad 28	Input "B"	V_{EE} −0.3	V_{CC5} +0.3	V
	Maximum Differential Voltage Input "A" to Input "B"	−1.0	1.0	V
Pad 3	TSEP OUT	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 4	"B"	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 5	TSEP IN Maximum Differential Voltage, "B" to TSEP IN or TSEP OUT	V_{EE} −0.3 −1.0	V_{CC5} +0.3 2.0	V V
Pad 6	V_{EE5}	−7.0	+0.3	V
Pad 7	"C"	V_{CC} −0.3	V_{CC5} +0.3	V
Pad 8	GA	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 9	BWLBLO	GND	+15	V
Pad 20	BWLALO	GND	+15	V
Pad 12	BWLAHI	V_{CC5}	+12	V
Pad 19	BWLBHI	V_{CC5}	+12	V
Pad 10	IS	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 11	GND	V_{EE} −0.3	V_{CC5} +0.3	V
Pad 13	OUT "B"	V_{CC5}	+25	V
Pad 14	OUT "A"	V_{CC5}	25	V

ABSOLUTE MAXIMUMS (cont)

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
Pad 15	V_{CC14}	V_{CC5} −0.3	25	V
Pad 16	V_{CC5}	V_{EE} −0.3	V_{CC14} +0.3	V
Pad 17	TA	V_{CC5}	V_{CC14} +0.3	V
Pad 18	415	GND −0.3	V_{CC5} +0.3	V
Pad 21	$V_{CC/2}$	GND	V_{CC5} +0.3	V
Pad 22	BWLO/O	−1	V_{CC5} +0.3	V
Pad 23	BF	−1	V_{CC5} +0.3	V
Pad 24	Bypass Common	V_{EE} −0.3	V_{CC5} +0.3	V

CAUTION NOTES:

1. **No input may fall below V_{EE5} −.3 to avoid latch-up and possible destruction.**
2. **All supplies should retain their relative polarities on power-up.**

TERMINAL IDENTIFICATION

PIN NUMBER	NAME	INPUT/OUTPUT	DESCRIPTION
1	Input A	Input	Main Signal Input Left
2	Input A	Input	Main Signal Input Left
3	TSEP OUT	Output	Trace Separation Buffer Out
4	B	Test	1st Stage Error Amp Bias Test Point
5	TSEP IN	Input	Trace Separation Buffer In
6	VEE5	Supply	Minus 5 V Supply
7	C	Input	Centering Input
8	GA	Input	Gain Adjust Input
9	BWLALO	Output	A Bandwidth Limit Filter Out
10	IS	Test	1st Stage Bias Test Point
11	GND	Supply	Ground
12	BWLA HI	Input	A Bandwidth Limit Filter Input
13	OUT A	Output	Main Stage Output Left
14	OUT B	Output	Main Stage Output Right
15	VCC14	Supply	+14.3 V Supply
16	VCC5	Supply	+5 V Supply
17	TA	Bias	Thermal Adjust Resistor Pad
18	415	Bias	Output Bias Current Setting Resistor
19	BWLB HI	Input	B Bandwidth Limit Filter Input
20	BWLB LO	Output	B Bandwidth Limit Filter Output
21	VCC/2	Test	1st Stage CB Stage Bias Test Point
22	BWL O/O	Input	Bandwidth Limit Mode On/Off
23	BF	Input	Beam Find Mode On/Off
24	Bypass Common	Bias	Optional Input Common Bypass
25	AUXOUT A	Output	Nonfunctional
26	AUX O/O	Input	Aux. Amp On/Off (Non-Functional)
27	Input B	Input	Main Signal Input Right
28	Input B	Input	Main Signal Input Right

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following operating conditions shall apply:

VCC14 (PAD #15) between 14 and 14.6 V
VCC5 (PAD #16) between 4.9 and 5.1 V
VEE5 (PAD #6) between −5.1 and −4.9 V
OUTA and OUTB (PADS #13 and 14) no lower than VCC14
R415 = 1700 Ω ± 1%
RTA = 2200 Ω ± 10%

PAD	SYMBOL	CONDITIONS	MIN	MAX	UNITS
1	I_{CCOUT}	+15 V DC Applied to Pins 13 & 14. Bias Current	109	132	mA
2	ICC14	+14 V DC Supply Bias Current (Pad 15)	Nominal	35	mA
3	ICC5	VCC5 Bias Current (Pad 16)	12	18	mA
4	IEE5	−5 V Supply Bias Current (Pad 6)	−80	−120	mA
6	IOBF	Output Current-Beam Find Zero Bias Current into either Output A or Output B with Beam Find Pin "HI"	29	105	mA
7	IIGA	Gain Adjust Bias Current Current Flowing into Gain Adjust Pin with V(GA)=VCC5	Nominal	40	μA
9	VIHBWL	BWL Gate Input Voltage Range (HI)	2.0	——	V
	VILBWL	BWL Gate Input Voltage Range (LO)	——	0.8	V

6

ELECTRICAL CHARACTERISTICS

PAD	SYMBOL	CONDITIONS	MIN	MAX	UNITS
10	IIHBWL	BWL Gate Input Bias Current (HI)	Nominal	10	μA
	IILBWL	BWL Gate Input Bias Current (LO)	——	−400	μA
11	VIHBF	Beam Find Input Voltage (HI)	2.4	——	V
	VILBF	Input Voltage (LO) (Pad 23)	——	0.8	V
12	IIHBF	Beam Find Bias Current (HI) Bias Current	Nominal	10	μA
	IILBF	(LO) Bias Current	0	−400	μA
13	IOMAX	Main Output Current Magnitude of Differential Output Current Output A to Output B (Pad 13 to Pad 14). Input Differential Voltage of 2 V applied to Pads 1 & 28. Beam Find Input LO.	42.2	51	mA
14	IOMAXBF	Main Output Current Same conditions as #14 with BF (Pad 23) HI.	3.0	25.2	mA
15	VOMAXTS	Trace Sep Control Voltage Output Voltage at Pad 3 with External Divider Network attached and +5 V and −5 V applied to Input Pad 5, respectively.	1.9	−.425	V
16	GMMMIN	Main Stage Gain VGA = 0 V Ratio of Diff. Output Current (Pad 13 to Pad 14) to the Diff. Input Voltage V(IN)A − V(IN)B (Pads 1, 2 to Pads 27, 28) 1 Div. deflection at Output Offset subtracted.	——	.166	MHO
17	GMMNOM	Main Stage Gain VGA = 2.5 V Same as #21 above	.166	.257	MHO

ELECTRICAL CHARACTERISTICS (cont)

PAD	SYMBOL	CONDITIONS	MIN	MAX	UNITS
18	GMMMAX	Main Stage Gain VGA = 5.0 V Same as #21 above	.257	——	MHO
19	IOC28+	Output Current Diff. Output Current Out. A Ref. to Out B GMM = .166 VC = 0 VIN = 0 (Pad 13 to Pad 14)	——	−4.7	mA
20	IOC28−	Output Current Diff. Output Current Out. A Ref to Out B GMM = .166, VC = −5 V, VIN = 0 V (Pad 13 to Pad 14)	4.7	——	mA
21	IOC43+	Output Current Diff. Output Current Out. A Ref to Out B GMM = .257, VC = 0 V, VIN = 0 V (Pad 13 to Pad 14)	——	−6.04	mA
22	IOC43−	Output Current Diff. Output Current Out. A Ref to Out B GMM = .257, VC = −5 V, VIN = 0 V (Pad 13 to Pad 14)	6.04	——	mA
23	AVTS	Trace Sep Gain Small-Signal Voltage Gain at TSEP OUT Referenced to TSEP In with a 500 Ω Load to Ground on TSEP Out and a 500 Ω Source Resistance	.92	1.00	——
24	AVBWL	Gain Change in BWL Mode. Ratio of Main Stage Gain w/BWL Input Low to Main Stage Gain w/BWL Input HI.	.986	.999	——

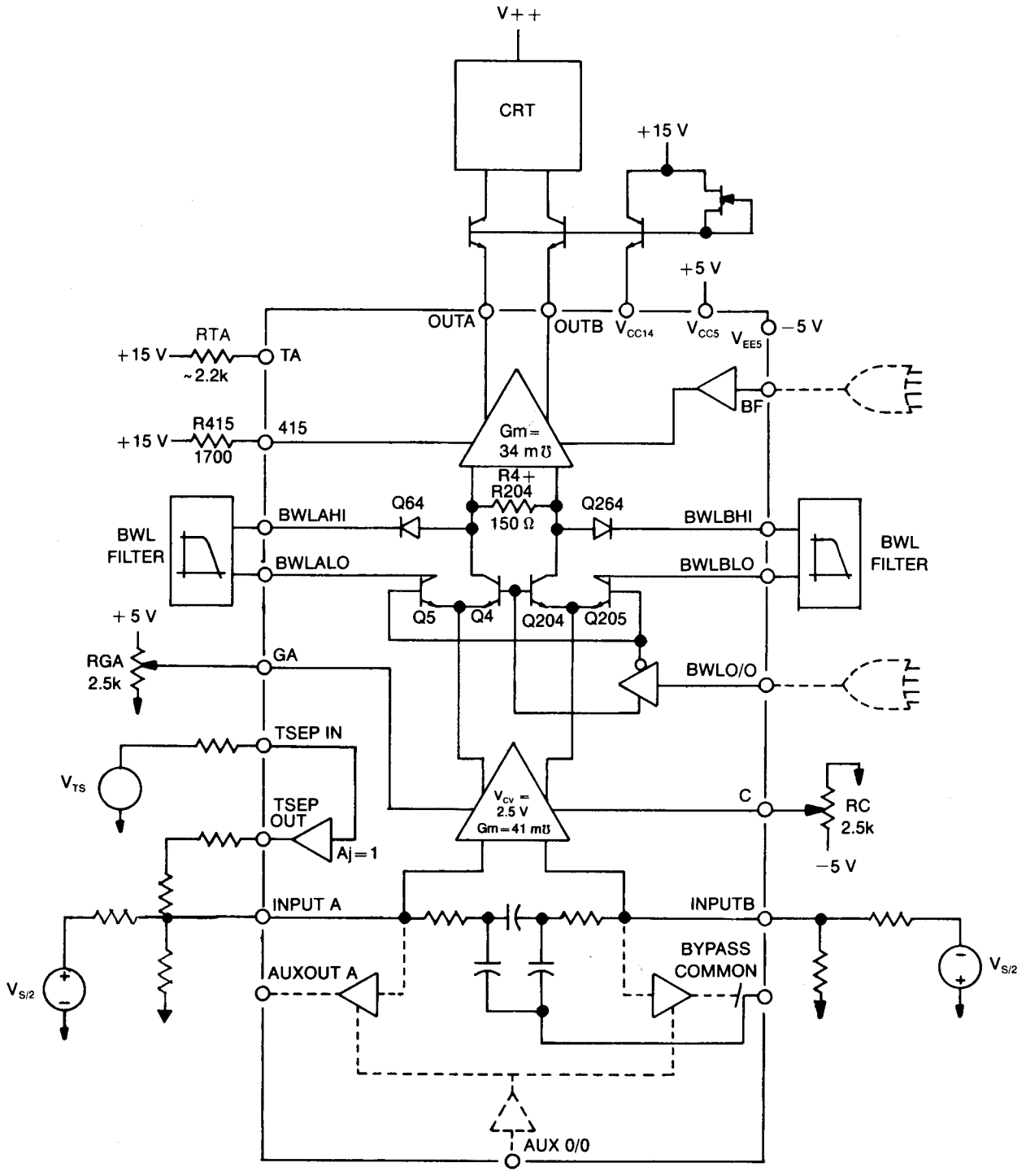
ELECTRICAL CHARACTERISTICS (cont)

PAD	SYMBOL	CONDITIONS	MIN	MAX	UNITS
25	LM	Main Stage Linearity. Ratio of the Differential Input Voltage causing a Diff. Output Current change from +3 Div to +4 Div (or −4 Div to +3 Div) to the Diff. Input Voltage causing a Diff. Output Voltage change from −1 Div to +1 Div.	.98	1.01	——
NOTE: Specifications 26 through 33 are guaranteed by the Fab Process and are not tested at Die Sort.					
26	ZBWL	BWLHI (1), BWLHI (2) Input Impedance. Small signal Low Freq Input impedance	70	90	Ω
27	ZINTS	Trace Separation small signal impedance	50	——	KΩ
28	IINTS	Quiescent Trace Separation Input Bias Current, VTS = 0	7.0	20.5	μA
29	ZINC	Centering Input Impedance	3.5	7.0	KΩ
30	VCOC	Open Circuit Centering Pad Voltage	−2.7	−2.3	V
31	ZINVCC/2	VCC/2 Input Impedance Small Signal	750	1300	Ω
32	VCC/20C	Open Circuit VCC/2 Pad Voltage	1.9	2.2	V
33	ZOBWLLO	Small Signal Differential Output Impedance, BWLALO to BWLBLO	20K	——	Ω

6

APPLICATION INFORMATION

203-0212 Block diagram showing typical application



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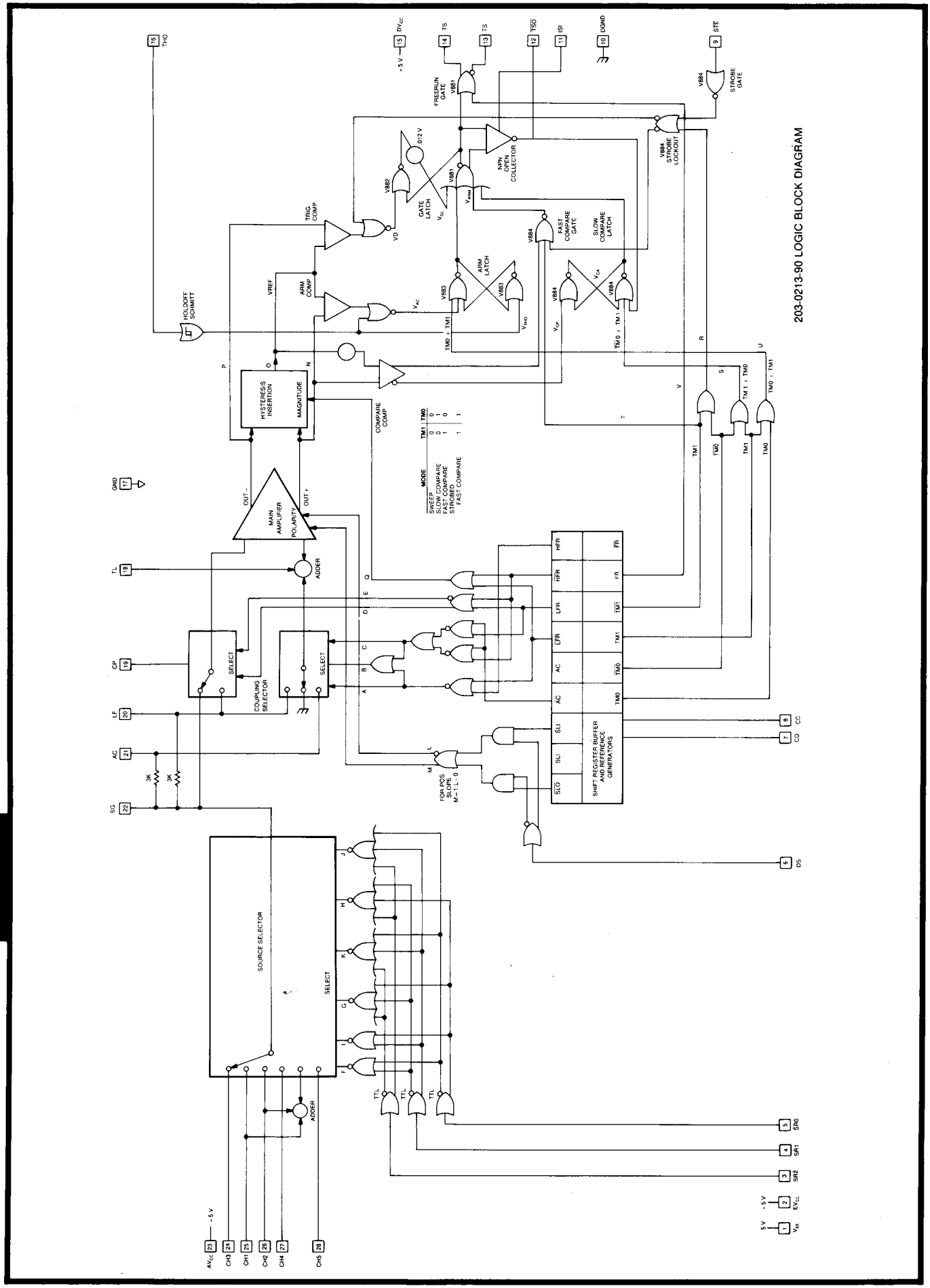
SHF III TRIGGER

DESCRIPTION

The 203-0213-90 die operates in several modes to provide sweep triggers or to shape the input for digital functions. It processes signals from DC to 600 MHz. The circuit dynamically selects the trigger sources in response to source code inputs. Slope, coupling, and mode are determined by a serially loaded control register.

- Bandwidth DC to 600 MHz
- 5 Signal Source Trigger Circuit (CH1-CH5)
- Control Register
- Signal Level Detection Modes
  - Sweep Trigger Mode
  - Slow Compare Mode
  - Fast Compare Mode
  - Strobed Fast Compare Mode


203-0213-90 LOGIC BLOCK DIAGRAM
TM0
HOLDOFF SCHMITT
TRIG COMP
ARM COMP
VREF
HYSTERESIS INSERTION
MAGNITUDE
COMPARE COMP
MAIN AMPLIFIER
POLARITY
OUT −
OUT +
ADDER
SELECT
COUPLING SELECTOR
SOURCE SELECTOR
TTL
GND
TL
CP
LF
AC
SG
3K
3K
TM1
TM0
MODE
SWEEP
SLOW COMPARE
FAST COMPARE
STROBED
FAST COMPARE
FREERUN GATE
V881
V882
V883
V884
GATE LATCH
ARM LATCH
FAST COMPARE GATE
SLOW COMPARE LATCH
NPN OPEN COLLECTOR
STROBE GATE
STROBE/HOLDOFF LOCKOUT
+5 V
TS
TSG
ISI
DGND
STE
SHIFT REGISTER BUFFER AND REFERENCE GENERATORS
LOW POS SLOPE M=1 L=0
CC
CD
DS
SR0
SR1
SR2
+5 V
EVCC
VEE
AVCC
CH3
CH1
CH2
CH4
CH5

ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	MIN	MAX	UNITS
T_J	Operating Junction Temperature	−25	+125	°C
T_{STG}	Storage Temperature	−50	+150	°C
	Digital Inputs With Common Parameters −CC, CD, −DS, −SR0, −SR1, −SR2			
	Safe Input Range	−0.3	(VCC5 +0.3)	V
	Maximum Bias Current	25	−250	μA
VCC5	Maximum Voltage Range	−0.3	+7.0	V
VEE5	Maximum Voltage Range	+0.3	−7.0	V
CH1, CH2, CH3, CH4, CH5	Maximum Voltage Range	——	±2.0	V

6

TERMINAL IDENTIFICATION

PAD	NAME	INPUT/OUTPUT	DESCRIPTION
1	VEE	SUPPLY	−5 Volt Supply
2	EVCC	SUPPLY	Extra Contact to DVCC
3	−SR2	INPUT	Not Bit 2 Source Select
4	−SR1	INPUT	Not Bit 1 Source Select
5	−SR0	INPUT	Not Bit 0 Source Select
6	−DS	INPUT	Not Delay Select
7	CD	INPUT	Control Data Input
8	−CC	INPUT	Not Control Clock Input
9	−STB	INPUT	Not Fast Compare Strobe
10	DGND	SUPPLY	Digital Ground
11	IST	——	External Pulldown to −5 Volts
12	−TSO	OUTPUT	Not Trigger Status Output
13	−TG	OUTPUT	Not Trigger Gate Output
14	TG	OUTPUT	Trigger Gate Output
15	DVCC	SUPPLY	Digital +5 Volts Supply
16	THO	INPUT	Trigger Holdoff
17	AGND	SUPPLY	Analog Ground
18	TL	INPUT	Trigger Level Input
19	CP	——	Compensation Capacitor
20	LF	——	LF Capacitor
21	AC	——	AC Capacitor
22	SS	OUTPUT	Source Selector Output
23	AVCC	SUPPLY	Analog +5 Volt Supply
24	CH3	INPUT	CH3 Input
25	CH1	INPUT	CH1 Input
26	CH2	INPUT	CH2 Input
27	CH4	INPUT	CH4 Input
28	CH5	INPUT	CH5 Input

TABLE 1
ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Trigger Source	Source Code Change To Corresponding Change In Trigger Selection	——	100	nS
Coupling	20 Hz Filter Cut Off Frequency	10	30	Hz
	50 Hz Filter Cut Off Frequency	36	70	kHz
	Residual Sinewave Amplitude	——	2	%
Slope Select	Time For Trigger Slope Selection to Change	——	10	nS
Trigger Level	Trigger Range	1.146	1.374	V
Trigger Level	Trigger Offset	——	±50	mV
Trigger Level	Trigger Gain Non-Linearity Effect On Trigger Level Max Sinewave Freq. Effect on Trigger Level	.99	1.01	
Trigger Level	DCN to 1 kHz	——	±1	%
	1 MHz to 50 MHz	——	+2 −10	% %
	50 MHz to 300 MHz	——	+2 −50	% %
Trigger Level	Trigger Hysteresis	5.25	8	mV
Trigger Level	Trigger Hysteresis Noise REJECT Selected	14	24	mV
Trigger Mode	Propagation Delay in SWEEP TRIGGER Mode	——	3	nS
Trigger Mode	Propagation Delay Variation SWEEP TRIGGER Mode (Jitter)	——	50	pS
Trigger Mode	Maximum Trigger Repetition Rate, SLOW COMPARE Mode	25	——	MHz
Trigger Mode	Maximum Trigger Repetition Rate, FAST COMPARE MODE	300	——	MHz

TABLE 1 (cont)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Trigger Mode	Maximum Trigger Repetition Rate, STROBED FAST COMPARE Mode	300	——	MHz
Trigger Mode	Minimum Time Trigger Strobe	——	2	nS
Digital Inputs SR0, SR1, SR2, −CC, −DS	VIL	−0.3	+0.8	V
Digital Inputs SR0, SR1, SR2, −CC, CD, −DS	VIH	+2.0	VCC5+0.3	V
Digital Inputs SR0, SR1, SR2, −CC, CD, −DS	Input Current	−10	+50	μA
Digital Inputs SR0, SR1, SR2, −CC, CD, −DS	Capacitance	——	5	pF
Digital Input THO	VIL	−0.3	VCC5 −1.675	V
Digital Input THO	VIH	VCC5 −1.035	VCC5 +0.3	V
Digital Input THO	IIH (Input Current)	−10	+50	μA
Digital Input −STB	VIL	−0.3	VCC5 −1.44	V
Digital Input −STB	VIH	VCC5 −1.035	VCC5+0.3	V
Digital Input −STB	Input Current	+10	−50	μA

TABLE 1 (cont)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Digital Input −STB	Capacitance	——	5	pF
Digital Input CD	Valid Data Set-up Time	0	——	nS
Digital Input −CC	−CC Pulse Width	300	——	nS
Digital Input −CC	−CC Hysteresis	0.1	——	V
Analog Input CH1, CH2, CH3, CH4, CH5	Input Current	−10	+25	μA
Analog Input TL	TL Input Resistance	2	3	KΩ
VCC5	Supply Current	90	180	mA
VEE5	Supply Current	−50	−100	mA
Output TG, −TG	VOL	3.1	3.38	V
Output TG, −TG	VOH	3.95	4.3	V
Output −TS	VOL	+0.1	−0.25	V
Output −TS	IOH	——	2	μA
Output −TS	IOL, Output Current For −TS V_{OUT} = 5 Volts	8.0	12.0	mA

6

Applications Information

TRIGGER FEATURES

The Trigger circuit has five signal sources (CH1, CH2, CH3, CH4, and CH5).

Dynamic trigger selection code signals (−SR0, −SR1, −SR2) determine the trigger sources:

−SR2	−SR1	−SR0	TRIGGER SELECTION
0	0	0	CH5
0	0	1	CH1
0	1	0	CH2
0	1	1	CH1 and CH2 (SUM)
1	0	0	CH5
1	0	1	CH3
1	1	0	CH4
1	1	1	CH1 and CH2 (SUM)

CONTROL REGISTER

Data shifts into the Control Register from the control input at not Control Clock Low to High Transitions, Bit 7 first and Bit 0 last. Active level is high at digital input.

BIT	FUNCTION
0	−TM0, Not Trigger Mode LSB
1	−TSM1, Not Trigger Mode MSB
2	−FR, Not Free Run, Continuous Trigger Gate
3	−HFR, Not Insert 50 kHz Low Pass
4	−LFR, Not Insert 50 kHz High Pass
5	−AC, Not Insert 20 Hz High Pass
6	SL1, Slope for Not Delay Select = 1
7	SL0, Slope for Not Delay Select = 0

TRIGGER SIGNAL COUPLING

The independently selected input for each trigger may be coupled to the trigger level comparator directly or through independently selected filters. Noise reject is actually an increased trigger hysteresis, rather than a filter. Control data inserts the filters.

AC	LFR	HFR	COUPLING SELECTED
0	0	0	Direct (DC)
0	0	1	50 kHz Low Pass (HFR)
X	1	0	50 kHz High Pass (LFR)
0	1	1	Direct, Noise Reject (DC NR)
1	0	0	20 Hz High Pass (AC)
1	0	1	20 Hz to 50 kHz Bandpass (AC HFR)
1	1	1	20 Hz High Pass Noise Reject (AC NR)

TRIGGER SLOPE SELECTION

Controlled by the Not Delay Select Inputs and Control Data

SL1	SL0	−DS	SLOPE
0	0	X	Positive
0	1	0	Negative
0	1	1	Positive
1	0	0	Positive
1	0	1	Negative
1	1	X	Negative

SIGNAL LEVEL DETECTION

Trigger Gate and Trigger Status Outputs represent the history of the difference voltage between the Selected Trigger Soruce and the Trigger Level. Trigger outputs respond to trigger signals according to the Trigger Hold-Off signal according to Trigger Slope, Control Data, and the Not Delay Select Input, and according to Trigger Mode Control data. TM0 and TM1 establish four modes of Trigger Circuit operation. The Trigger Gate Output (TG) is continuously true when the Free Run Control Bit FR is true.

SIGNAL LEVEL DETECTION (cont)

TM1	TM0	TRIGGER MODE SELECTION
0	0	**SWEEP TRIGGER MODE** The Trigger Gate sets at the first crossing of the Trigger Level by the Trigger Signal in the direction of the Selected Slope after the Trigger Signal is displaced in the opposite direction in the absence of Trigger Holdoff. The Trigger Gate resets at the assertion of Trigger Holdoff.
0	1	**SLOW COMPARE** The Trigger Gate sets when the Trigger Status Output has recovered to the false state, and the Trigger Signal is displaced from the Trigger Level in the direction of the selected slope. The Trigger Gate resets when the Trigger Signal is displaced from the Trigger Level in the opposite direction of the selected slope.
1	0	**FAST COMPARE MODE** The Trigger Gate sets when the Trigger Signal is displayed from the Trigger Level in the direction of the selected slope and resets when the Trigger Signal is displaced in the opposite direction.
1	1	**STROBED FAST COMPARE MODE** The Trigger Gate sets when the Trigger Strobe is true and the Trigger Signal is displaced from the Trigger Level in the opposite direction of the selected slope. The Trigger Gate resets when the trigger signal is displaced in the opposite direction.

Trigger Status corresponds directly to Trigger Gate except that Free Run has no effect on Trigger Status and that the Propagation Delay from the Trigger Gate True-to-False transition to the True-to-False transition of Trigger Status output is primarily determined by external circuitry. This enables slower external circuits to respond to very fast trigger events. Internally the Slow Compare Mode cycle rate is limited by the externally determined propagation time of the Trigger Status Output.

In the direction of the Selected Slope, the Trigger Gate resets when the Trigger Strobe is True and the Trigger Signal is displaced.

6

RELIABILITY

λ, Failure rate $\leq$0.02%/1000 hours at 75°C Tj

SWEEP INTEGRATOR DIE

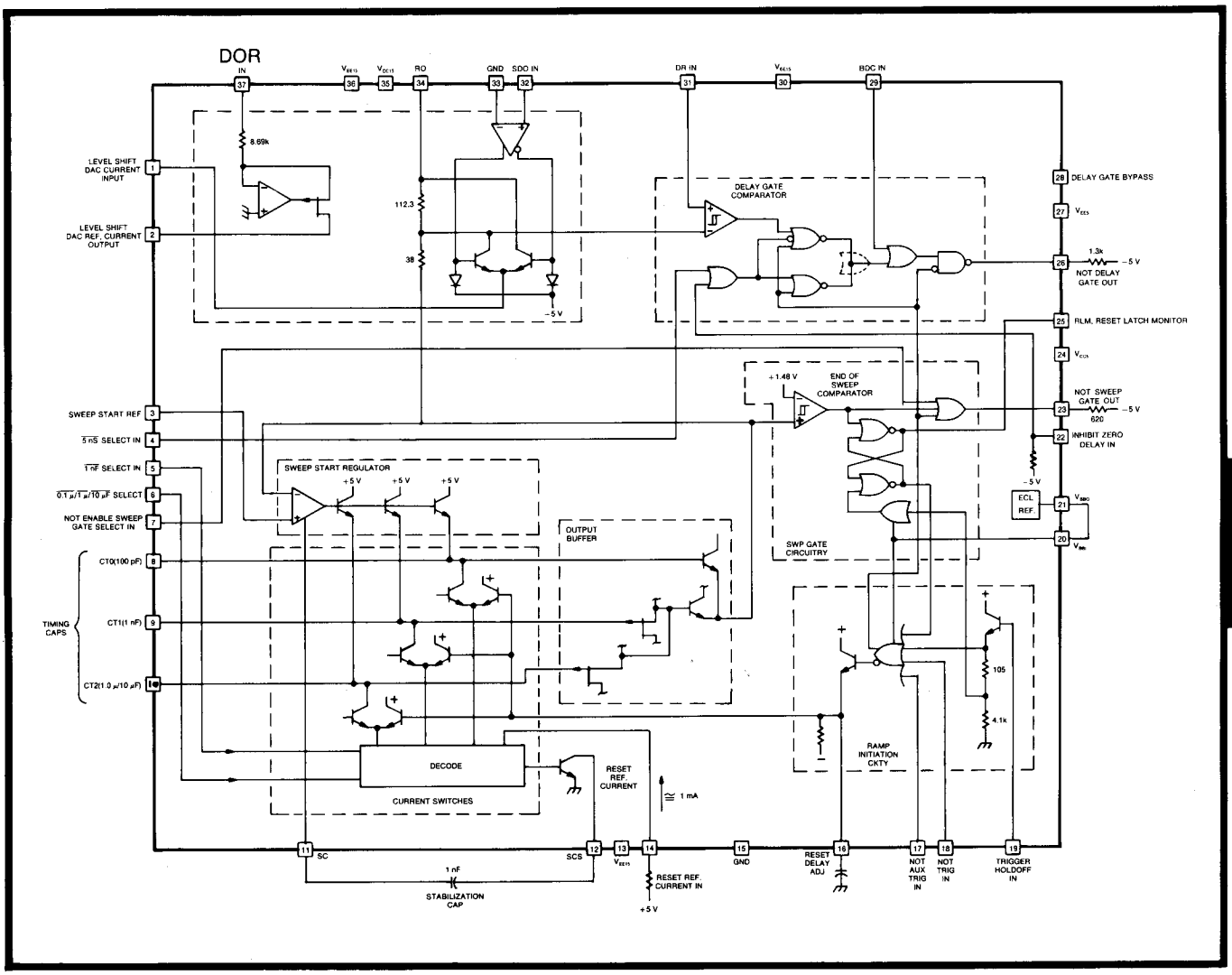
DESCRIPTION

The 203-0214-90 is part of a Sweep Gate Circuitry, Integrator Current Switches, Sweep Start Regulator, Delay Gate Comparator, Ramp Output Buffer, and a portion of the Sweep Display Delay Circuitry.

When used with the 203-0231-90, a complete Sweep Circuit system is generated with very few external components.

FEATURES

- Ramp Initiation Sweep Gate Circuitry
- Integrator Current Switches
- Sweep Start Regulator
- Delay Gate Comparator
- Buffered Ramp Output
- Sweep Display Delay Circuitry
- 200 Ω/Sq. BIFET process
- Max sweep speed 5 nS/Div (2.5 V Ramp)
- For electrical characteristics contact Applications Engineering



ABSOLUTE MAXIMUMS

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
T_J	Operating Junction Temperature	−15	+115°C	°C
T_{STG}	Storage Temperature	−55	+150	°C
Pad 35	VCC15 +15 V Voltage Range	VCC5 −0.3	+18	V
Pad 24	VCC5 +5 V Voltage Range	−0.3	+7.0	V
Pad 27	VEE5 −5 V Voltage Range	−7.0	+0.3	V
Pad 13, 30, 36	VEE 15 −15 V	−18	VEE +0.3	
Pad 1	Level Shift DAC Current Input	−10	0.0	mA
Pad 2	Level Shift DAC Reference Current Out Voltage Range at Pad	+0.3	VEE5	V
Pad 3	Sweep Start Reference in Voltage Range at Pad	−3.5	+2.0	V
Pad 4	Not 5 nS in Voltage Range at Pad	−0.3	VCC5 +0.3	V
Pad 5, 6	Not 1 nF Select In Not 0.1 μF, 1 μF, 10 μF Select In Voltage Range at Pad	−0.3	VCC5 +0.3	V
	Maximum Voltage Difference Between Pads	——	6.0	V
Pad 7	Not Enable Sweep Gate Voltage Range at Pad	−0.3	VCC5 +0.3	V

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ABSOLUTE MAXIMUMS (cont)

SYMBOL	IDENTIFICATION	MIN	MAX	UNITS
Pad 8, 9, 10	Timing Cap Ports	Refer to Note #1		
Pad 17, 18	Not Aux Trigger In Not Trigger In Voltage Range at Pads	0.0	Note #2	V
Pad 19	Trigger Holdoff In Voltage Range At Pad	−0.3	VCC5 +0.3	V
Pad 20	VBB In Voltage Range at Pad	−0.3	VCC5 +0.3	V
Pad 22	Inhibit Zero Delay in Voltage Range at Pad	VEE5 −0.3	VCC5 +0.3	V
Pad 23	Not Sweep Gate Out Current Out of Pad	−15	0	mA
Pad 26	Not Delay Gate Out Current Out of Pad	−10	0	mA
Pad 29	Bypass Delay Comparator in Voltage Range at Pad	−0.3	VCC5 +0.3	V
Pad 31	Delay Reference in Voltage Range at Pad	VEE5	VCC5	V
Pad 32	Sweep Delay Offset Reference in Voltage Range at Pad	−3.5	+3.5	V
Pad 37	Delay Offset Reference In	VEE15	VCC15	V

NOTE #1: With VCC5 regulating (VCC5 = 5.0 V ±3%) and the voltage at SSR between −1.2 and −1.3 V, the following limits MUST be observed:

—Minimum voltage that may be applied to a selected timing capacitor port:

Pad 8..... +1.1 V
Pads 9/10..... +0.6 V

—Minimum voltage that may be applied to an unselected timing capacitor port:

Pads 8/9/10 ..... −0.8 V

—Maximum voltage that may be applied to the timing capacitor ports is VCC5 +0.3 V.

NOTE #2: Maximum voltage at "not Trigger" and "Auxiliary Trigger" inputs is VCC5 +0.3 V OR 6.5 V whichever is the smaller.

CAUTION NOTE: The Not 1 nF Select Input (Pad 5) and/or the Not 0.1/1/10 μF Select Input (Pad 6) MUST NOT be left open with the power supplies on.

TERMINAL IDENTIFICATION

PAD #	NAME	INPUT/OUTPUT	DESCRIPTION
1	LSDC	Input	Level Shift DAC Current
2	LSDRC	Output	Level Shift DAC Ref. Current
3	SSR	Input	Sweep Start Reference
4	Not 5 nS	Input	Not 5 nS Select In
5	Not 1 nF	Input	Not 1 nF Select In
6	Not 0.1 μ/1 μ/10 μF	Input	Not 0.1 μF/1 μF/10 μF Select In
7	Not ESG	Input	Not Enable Sweep Gate Select In
8	CT0 (100 pF)		Timing Cap
9	CT1 (1 nF)		Timing Cap
10	CT2 (0.1 μ/1 μ/10 μF)		Timing Cap
11	SC		Stabilization Cap
12	SCS	Output	Stabilization Capacitor Select
13	VEE15	Supply	−15 V Supply
14	ER	Input	Reset Ref. Current In
15	GND		Ground
16	RDA	Input	Reset Delay Adjust
17	Not Aux Trig	Input	Not Auxiliary Trigger In
18	Not Trig	Input	Not Trigger In
19	THO	Input	Trigger Holdoff In
20	VBBI	Input	VBB (ECL Reference) In
21	VBBO	Output	VBB (ECL Reference) Out
22	IZD	Input	Inhibit Zero Delay In
23	Not SG	Output	Not Sweep Gate Out
24	VCC5	Supply	+5 V Supply
25	RLM	Output	Sweep Reset Latch Monitor
26	Not DG	Output	Not Delay Gate Out
27	VEE5	Supply	−5 V Supply
28	DGB	Input	Delay Gate Bypass
29	BDC	Input	Bypass Delay Comparator In
30	VEE15	Supply	−15 V Supply
31	DR	Input	Delay Reference In
32	SDO	Input	SWP Display Offset Ref. In
33	GND		Ground
34	RO	Output	Ramp Out
35	VCC15	Supply	+15 V Supply
36	VEE15	Supply	−15 V Supply
37	DOR	Input	Delay Offset Ref. In

APPLICATIONS INFORMATION

Ramp Initiation Sweep Gate Circuitry

Ramp is initiated by the coincidence of a "LO" at the "Not Trigger", "Not Auxiliary Trigger" and "Trigger Holdoff" inputs. Operation corresponding to this set of inputs will be called "Sweep" in future paragraphs. Note that for the 203-0214-00 to ramp by itself (without the aid of the 203-0231-00), one of the three timing capacitor ports must be selected using the procedure given in Table 1, an appropriate capacitor attached to the selected port and an appropriate current source also attached to that port.

If the "Not Enable Sweep Gate" input is "LO", the "Not Sweep Gate" output will be "LO" during "Sweep". If the "Not Enable Sweep Gate" input is "HI", the "Not Sweep Gate" output will always remain "HI".

APPLICATIONS INFORMATION (cont)

Ramp is terminated when the internal ramp reaches the End-Of-Sweep threshold (approximately 1.48 V) or when "Trigger Holdoff" is asserted ("HI" at THO input). At termination, the "Not Sweep Gate" output will go "HI" and the internal ramp will return to the Sweep Start voltage. This sequence is called "Reset". Ramp termination may be delayed, relative to the "Not Sweep Gate" output ("LO" to "HI" transition) by attaching a capcitor to Pad 16 (Reset Delay Adjust RDA). This feature allows the Z-Axis time to blank the CRT before the ramp starts to slow down.

A latch is provided and functions such that when the internal ramp reaches End-Of-Sweep voltage, the latch is set holding the 203-0214-00 in the "Reset" condition. The latch is reset when "Trigger Hold-Off" goes "HI". At this point, the "HI" at "Trigger Hold-Off" maintains the 203-0214-00 in the "Reset" condition. In this manner, the time from "Not Sweep Gate" output "LO" to "HI" transition until "Trigger Hold-Off" input "LO" to "HI" transition can be long allowing for substantial delay through the scope logic circuitry.

Ramp Initiation Sweep Gate Circuitry

The internal latch does result in a potential logic trap. After an internal reset "Not Trigger", "Not Auxiliary Trigger" and "Trigger Hold-Off" can all be "LO" and the circuit may not ramp. "Trigger Hold-Off" must always go "HI" (after an internal reset) to clear the latch before the circuit can ramp again.

The internal ramp voltage (mentioned above) differs from the ramp out voltage by the amount of level shift/offset in effect at that specific sweep. Refer to Section on "Sweep-Display Delay Circuitry".

Integrator Current Switches

There are three current switches in the 203-0214-00 (one for each timing cap port). Only the current switch corresponding to the selected timing capacitor is active. The tail current to the other two current switches is "0". The tail current to the active current switch is always greater than the maximum timing current. During "reset", the current available to discharge the timing capacitor is equal to the current switch tail current minus the timing current. When the internal ramp reaches the sweep start voltage (during "Reset"), the "Sweep Start Regulator" supplies this differential current. Refer to section on Sweep Start Regulator.

During "Sweep", the current switch tail current is switched into a supply, allowing the timing current to flow into the timing cap.

Sweep Start Regulator

During "Reset" this circuit maintains the voltage at the internal ramp output equal to the voltage present at the "Sweep Start Reference (SSR)" input. SSR voltage may range from -1.2 to -1.3 V. Stability of this feedback circuit is insured, for the 100 pF and 1 nF timinig capacitor case, by switching in a 1 nF stabilization capacitor putting a dominant pole near the input portion of the "Sweep Start Regulator" circuitry. When the 0.1/1/10 μF timing capacitor is slected, the stabilization cap is switched out and the 0.1/1/10 μF timing cap becomes the dominant pole.

During "Sweep" this circuitry is inhibited.

APPLICATIONS INFORMATION (cont)

Delay Gate Comparator

Normal operation of this circuit occurs when the "IZD" input is open, the "BDC" input is "LO" and the "Not 5 ns" input is "HI" for all sweep speeds (except 5 nS/Div where it is "LO"). Under these conditions, the "Not Delay Gate" output will remain "HI" until the internal ramp voltage (at the pickoff) becomes more positive than the voltage on the "Delay Reference (DR)" input. When the voltage becomes more positive, the "Not Delay Gate" will go "LO". The comparator is gated such that the function described above can only occur during "Sweep". Delay gate operation is controlled by the "DR" input at all sweep speeds (except the fastest (5 ns/Div—"NOT 5 nS input "LO").

At 5 nS/Div, the comparator gating function is modified such that "Not Delay Gate" will go "LO" immediately ("Zero Delay") after "Not Sweep Gate" goes "LO", regardless of the voltage at "DR". In a two sweep system this "Zero Delay" feature forwards or "pipes" the "Sweep" command through "A" Sweep to "B" Sweep allowing "B" Sweep to be used as the main sweep at 5 nS/Div. Use of "B" Sweep (at 5 nS/Div) may be desirable because the System Delay Constraints may result in excessive preview time if "A" Sweep were used. The "Zero Delay" feature may be inhibited by putting the "Inhibit Zero Delay (IZD)" input "HI" thus allowing the "DR" input to control the delay gate operation at all sweep speeds.

If the "Bypass Delay Comparator (BDC)" input is "HI", "Not Delay Gate" will go "LO" immediately after "Not Sweep Gate" goes "LO" regardless of the voltage at "DR", "IZD" input or any sweep speed related input ("Not 5 nS, Not 1 nF Select", etc.). "BDC" is used in "B" Sweep to assure that there is a "Gate" available coincident with "B" Sweep regardless of the setting at the "Not Enable Sweep Gate" input. The "Gate" (of course) appears at the "Not Delay Gate" output. In "A" Sweep, "BDC" is used in conjunction with the "Delay by Events" option and provides a fast path from trigger through the sweep.

"Not Delay Gate" will always go "HI" at the initiation of "Reset".

Buffered Ramp Output

Timing cap voltage is buffered by this circuitry consisting of FET source followers and/or NPN emitter followers. Voltage gain through this circuit is one (1), although there are DCN offsets due to the NPN emitter followers.

6

Buffered outputs from the three timing capacitors are merged at this point. How this is done can best be understood by referring to the Block Diagram or the schematics. When a capacitor is selected, it is necessary, for proper operation, to put the other two (off) timing cap ports at an appropriate voltage. This is normally done by the 203-0231-00. If the 203-0214-00 is to be operated by itself, reference should be made to Table 1 for the appropriate voltages.

Sweep Display Delay Circuitry

The Sweep Start Voltage, at "Ramp Out" is offset from "SSR" in proportion to Sweep Speed Setting, the "DOR" input voltage and the "DO" input voltage. Internally, the ramp applied to the delay comparator is offset in proportion to sweep speed setting and "DOR" input voltage. These offsets will result in a delay, since the ramp must run for a period of time before the "Ramp Out" voltages reaches the on screen voltage (approximately SSR) or the ramp voltage applied to the pickoff comparator reaches the available delay comparator range. Because the offsets are in proportion to the sweep speed setting, the delay will be constant for all sweep speeds. Also "DOR" is ganged with the timing reference voltage, so the delay will remain constant even when variable is operated. The delays due to these offsets are about 6 nS at the comparator pickoff point and a maximum of about 20 nS at "Ramp Out". Additionally, by operating "SDO", the delay at "Ramp Out" may be varied from about 20 nS to 10 nS.

APPLICATIONS INFORMATION (cont)

Offsetting is done for sweep speeds of 500 nS/Div or faster. Sweep speeds of 1 μS/Div and slower have no offset.

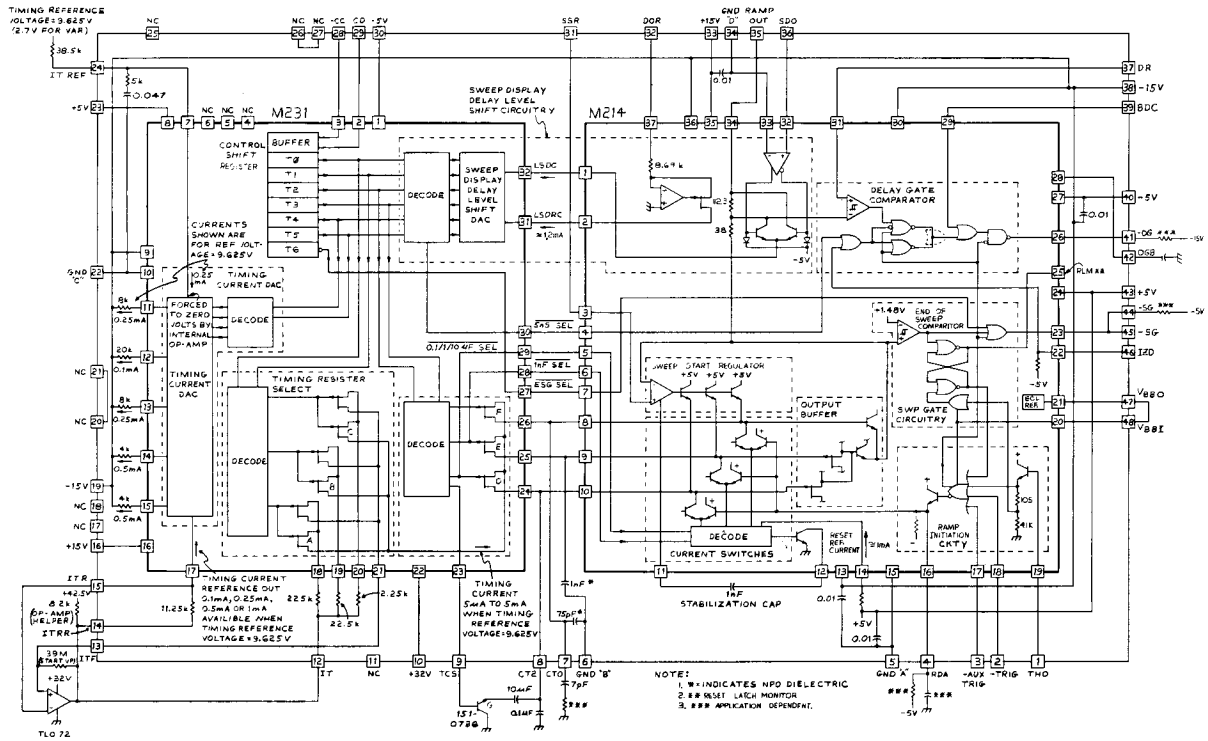
Offset/Delay is used for the following purpose:

— Provide time for the ramp to become linear before it reaches on screen voltage and before it reaches available delay pickoff comparator stage.

— Maintains the unblanked, linear start of the displayed sweep at a nearly constant position for all sweep speeds.

— Allows "A" Sweep delay to be made longer than "B" Sweep delay so that in "B" Starts After Delay scope operating mode, the trigger edge may be viewed with "B" Sweep.

Level shifting is accomplished by passing a current through two series resistors hooked between the ramp buffer and "Ramp Out". The current comes from a DAC (in the 203-0231-00) which is programmed by a control register containing the Sweep Speed information. The reference current for the DAC is proportional to "DOR" and comes from the 203-0214-00 since it must also be related to the sheet resistance of the two level shift resistors. A gain cell, operated by "SDO", proportions the "Ramp Out" offset, but does not affect the offset at the delay pickoff comparator.



6

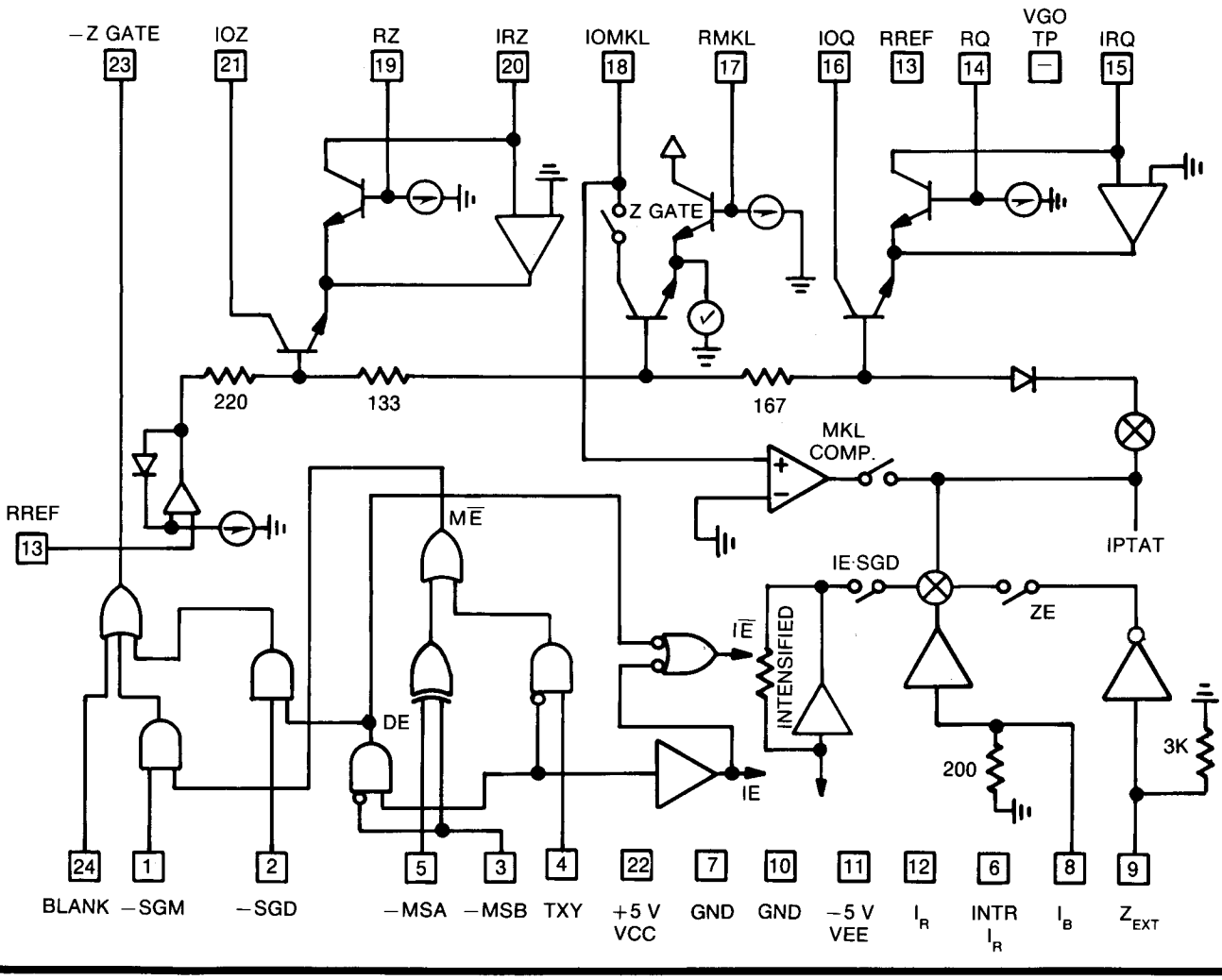
AUTOFOCUS PROCESSOR DIE

DESCRIPTION

The function of this circuit is to process the various intensifying inputs and to generate an appropriate focus function for the MSE type of CRT. Since the perceived intensity of the CRT spot light source is logarithmic and the transfer function from the bright intensity input to the grid drive output is exponential, the resultant perceived transfer function is made linear.

- SHF-III Process
- High f_t at low currents
- Low R_b and R_e for predictable exponential characteristics
- 50 Ohm NiCr Resistors
- Cost effective focus correction for M.S.E. CRT's.

BLOCK DIAGRAM



ABSOLUTE MAXIMUMS

		VALUE		
SYMBOL/PINS	IDENTIFICATION	MIN	MAX	UNITS
T_J	Operating Junction Temperature	−15	+115	°C
T_{STG}	Storage Temperature	−60	+125	°C
Pads 1,2,3,4,5, 6,12,15,16, 18,20,21,24	Maximum Input Voltage	−0.3	VCC +0.3	V
Pad 8	Bright Input Current	−2.0	+2.0	mA
Pad 9	External Z-Axis Maximum Input Current	−20.0	+20.0	mA
Pad 11	VEE Voltage	−7.0	+0.3	V
Pads 14,17,19	Adjust Inputs	−0.3	+0.3	V
Pad 22	VCC Voltage	−0.3	+7.0	V
Pad 23	−ZGATE Output Maximum Output Loading		−3.0	mA

CAUTION NOTES:

This product is sensitive to static charges and care should be taken in handling. Pins interfacing directly to transistor bases are most critical.

6

CAUTION

This product is sensitive to static charges.

TERMINAL IDENTIFICATION

PAD #	NAME	INPUT/OUTPUT	DESCRIPTION
1	−SGM	Input	Main Sweep Gate
2	−SGD	Input	Delayed Sweep Gate
3	−HSB	Input	Horizontal Select B
4	TXY	Input	Horizontal Mode XY Logic Triggered XY Mode
5	−HSA	Input	Horizontal Select A
6	IIZ	Input	Intensified Zone Reference Current
7	GND	Supply	Analog Ground
8	IB	Input	Bright Current
9	EXTZ	Input	External Z Current
10	GND	Supply	System Ground
11	VEE	Supply	−5 V Supply
12	IR	Input	1.0 mA Reference Current
13	RREF	Input	ADJ Reference Register
14	RQ	Input	Q Output Calibration Resistor
15	IRQ	Input	Q Output Reference Current
16	IDQ	Output	Q Exponential Current
17	RMKL	Input	MKL Calibration Resistor
18	IOMKL	Output	MKL Exponential Current
19	RZ	Input	Z Output Calibration Resistor
20	IRZ	Input	Z Output Reference Current
21	IOZ	Output	Z Exponential Current
22	VCC	Supply	+5 V Power Supply
23	−ZGATE	Output	ZGate Logic
24	BLANK	Input	Blank Gate

ELECTRICAL CHARACTERISTICS

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
1	ICC	Positive Supply current All Logic Inputs = "HI" IB = 0 VCC = 5.0 V	42	54	mA
2	IEE	Negative Power Supply All Logic Inputs = "HI" IB = 0 VEE = −5.0 V	−62	−46	mA
3	VR	IR Input Voltage IREF = 0.9 mA	−2.0	−1.0	V
4	VRZ	IRZ Input Voltage IRZ = 1.25 mA IB = 0	−250	−0	mV
5	VRQ	IRQ Input Voltage IRQ = 0.481 mA IB = 0	−250	−40	mV
6	RZ	Z Adjust Resistance IOZ = 5.0 mA, IRZ = 1.25 mA IB = 1.0 mA, RREF = 90 Ω Pad to Gnd Resistance to obtain indicated current.	65	100	Ω
7	RMKL	MKL Adjust Resistance IOZ = 2.31 mA, RMKL = 50K to VCC IB = 1.0 mA, RREF = 90 Ω Pad to Gnd Resistance to obtain indicated current.	40	90	Ω
8	RQ	Q Adjust Resistance IOQ = 1.923 mA, IRQ = 0.481 mA IB = 1.0 mA, RREF = 90 Ω Pad to Gnd Resistance to obtain indicated current.	70	100	Ω
9	RIB	Brite Input Resistance	150	250	Ω
10	RIZ	External Z Input Resistance	2.3	3.7	KΩ
11	IIH	Logic High Input Current VIH = 5.0 V		20	μA

ELECTRICAL CHARACTERISTICS (cont)

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
12	IIL	Logic Lo Input Current VIL = 0 V BF and Blank Inputs	−100		μA
13	IIL	Logic Lo Input Current VIL = 0 V All Remaining Logic Inputs	−20		μA
14	VIH	Valid Range High Data	1.97	VCC +0.3	V
15	VIL	Valid Range Lo Data	−0.2	0.8	V
16	VOH	−ZGate Hi Output IL = 0.5 mA	1.8	2.2	V
17	VOL	−ZGate Lo Output IL = 0.5 mA	0.6	1.0	V
18	IOZM	Minimum IOZ IB = 0	0	30	μA
19	IIB	Full Scale Brite Input	0.665	0.785	mA
20	IIBRO	Readout Brite Input Current IOZ = 0.923 mA	0.44	0.54	mA
21	AIOZI	Z Output Intensified Zone Ratio Of $\frac{IOZI}{IOZh}$ IOZI = Value of IOZ with DSG low in main sweep mode and IOZh = Value with DSG high at the same value of IBrite, IOZI < 5.0 mA	1.60	2.10	A/A
22	AIEZ	External Z Axis Gain Equivalent to the change in IBrite divided by the change in IEXT Z that maintains IOZ at the same Ratio of IOZ with EXT Z amp on to IOZ with EXT Z amp off. IOZ = 1 mA.	−4	−7	A/A

ELECTRICAL CHARACTERISTICS (cont)

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
23	IOMKLLIN	MIL Output Linearity Difference between the IOMKL minus the 5/3 power of the IOZ. MKLLIN = IOMKL − k (IOZ)$^{5/3}$ where: k = IOMKLfs/(IOZfs)$^{5/3}$ and fs = full scale outputs		±50	μA
24	IOQLIN	Q Output Linearity Difference between the IOQ minus the 2.4 power of the IOZ QLIN = IOQ −k (IOZ)$^{2.4}$ where k = IOQfs/(IOZfs)$^{2.4}$ fs = full scale outputs		±0.05	mA
25	td	Fast Logic Input to ZGate Delay Time		2	nS
26	td	Slow Logic Input to ZGate Delay. Slow inputs are: −HSA −HSB TYY BF		100	nS
27	tdINT	Intensified Zone Delay Delay Time of Intensified Zone is the delay from †r - of DSG to 50% of IOZ		5	nS
28	tdEXTZ	External Z Transition Time		10	nS

6

APPLICATIONS INFORMATION

This circuit has a peak current gain of 50 at full scale output from the Bright Input and a gain of 300 from the EXTZ input. The bandwidth of 30 MHz results in a gain-bandwidth product of 9000 MHz.

Feedback from the exponential outputs to the inputs must be minimized to prevent oscillations and preserve transient response fidelity. The power supplies are also sensitive and must be bypassed with low inductance capacitors.

The RREF resistor determines the center value of the ADJ resistors. The value also affects the temperature drift of the outputs due to base current change with temperature.

The beam find function is not specified and that pin should be grounded to ensure remaining circuit functionality.

H.V. TRANSRESISTANCE AMP

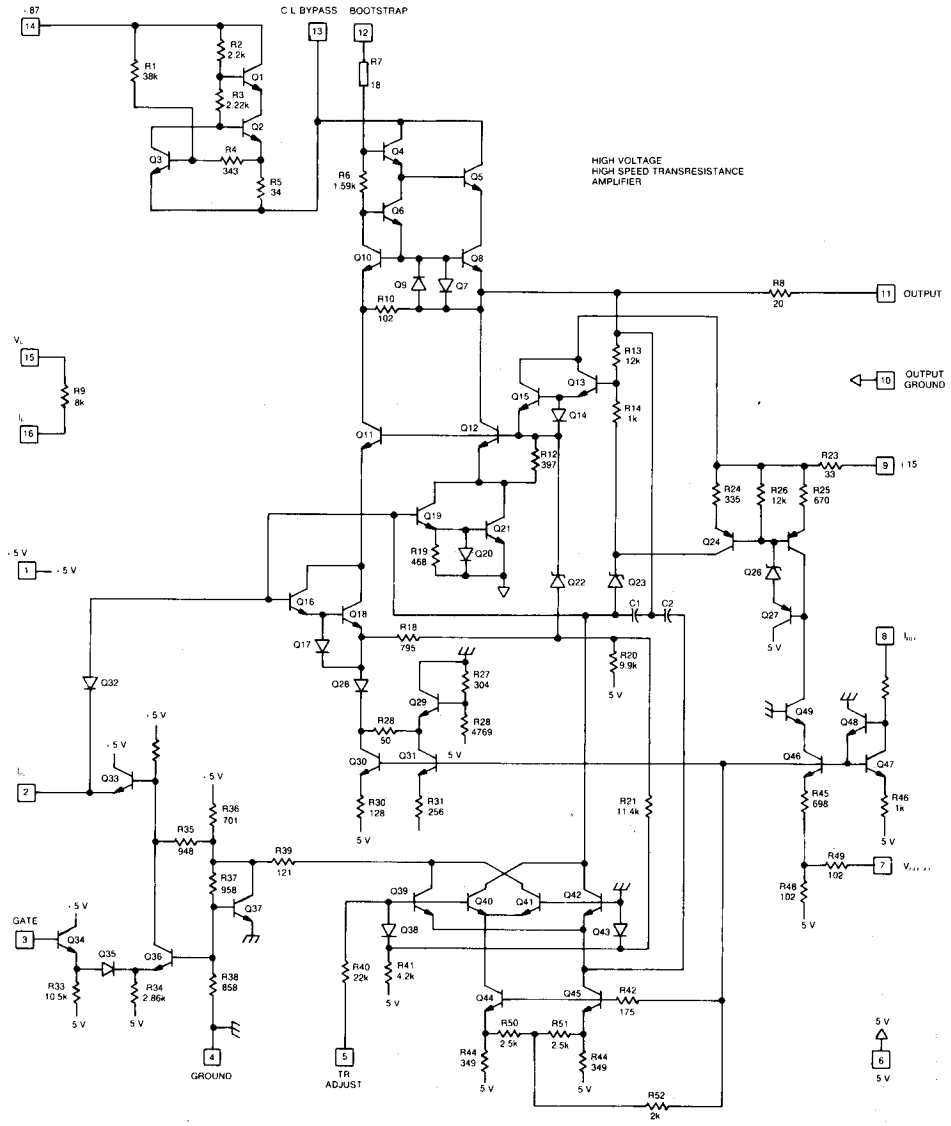
DESCRIPTION

The 203-0227-90 is a shunt feedback gated amplifier designed to drive capacitive loads. The SHHV process is utilized to obtain a BV(CBO) of 65 V and an F_t of 2 GHz.

FEATURES

- SHHV process
- Class AB amplifier
- All NPN output configuration
- 67 V dynamic output
- 15 ns risetime (22 pF load)
- 2 GHz F_t

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUE	UNITS
T_J	Operating Junction Temperature	−15 to +115	°C
T_{STG}	Storage Temperature	−60 to +125	°C
Pad 1	VCC5, +5 V Supply	−0.3 to +7.0	V
Pad 2	IIN, Max Voltage Range	−0.3 to +3.0	V
Pad 2	IIN, Max Current Range	−10 to 0	mA
Pad 3	Gate, Max Voltage Range	VCC −0.3 to +0.3	V
Pad 5	TR Adj, Max Voltage Range	−3.0 to +20	V
Pad 6	VEE, Max Voltage Range	−7.0 to −0.3	V
Pad 7	Offset Adj, Max Voltage Range	−15 to VCC15 +0.3	V
Pad 8	IREF, Max Voltage Range	VEE −0.3 to 0.3	V
Pad 9	VCC15, Max Voltage Range	−0.3 to +20.0	V
Pad 12	Bootstrap, Max Current Range	0 to +15.0	mA
Pad 13	CL Bypass, Max Voltage Range	VCC87 −.3 to 0	V
Pad 14	VCC87, Max Voltage Range	−0.3 to +95.0	V
Pad 15	VREF, Max Voltage Range	−15.0 to +15.0	V
Pad 16	IREF, Max Voltage Range	−15.0 to +15.0	V

TERMINAL IDENTIFICATION

PAD #	NAME	INPUT/OUTPUT	DESCRIPTION
1	VCC5	Supply	+5 V Supply
2	IIN	Input	Input Current to Amplifier
3	Gate	Input	TTL Not Gate
4	Ground	——	Input Ground
5	TR Adj	Input	Trans Response Voltage Adj
6	VEE	Supply	−5 V Supply
7	VOFF	Input	Quiescent Level Offset Adj
8	IREF	Input	Ref Current for Current Sources
9	VCC15	Supply	+15 V Supply
10	OUT GND	Ground	Output Ground
11	VO	Output	Amplifier Output
12	BS	Input	Bootstrap
13	CL	Output	Current Linearity Bypass
14	VCC87	Supply	+87 V Supply
15	VR	Input	Reference Voltage
16	IR	Output	Reference Current for Input

PARAMETRIC SUMMARY

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
1	ICC87	VCC87 source current includes current in external pullup. IIN = 0 mA	8.0	10.0	mA
2	ICC87	VCC87 short current IIN = 5 mA	16.0	27.0	mA
3	ICC15	VCC15 source current IIN = 0 mA	5.4	7.6	mA
4	ICC5	VCC5 source current	6.4	10.6	mA
5	IEE5	VEE5 source current	19.0	30.0	mA
6	I10	Reference current VREF = 10 V	1.0	1.5	mA
7	VOLO	Output Voltage, Low IIN = 0 mA VOFFSET = Open	9.0	13.0	V
8	VOLS	Output Voltage IIN = 0 mA VOFFSET = VEE	7.0	11.0	V
9	VTR+	Output Voltage Change IIN = 0 mA VTR = 7.5 to 15 V	0	±.55	V
10	VTR−	Output Voltage IIN = 0 V VTR = 7.5 to 0 V	0	±0.55	V
11	VBS	Bootstrap Output Voltage IIN = 0 mA, with respect to VOLS	9.5	16.5	V
12	VIN	IIN Pad input voltage IIN = 10 mA VGATE = 2.0 V	0.95	1.35	V
13	VIN	IIN Pad input voltage IIN = 5 mA VGATE = 1.0 V	0.3	0.8	V
14	VOH	Output Voltage, HI IIN = 4IR	VOLS +62.0	VOLS +67.0	V

CONDITIONS FOR PARAMETERS 15 THROUGH 19
ADJUST IIN0 FOR VOUT = 65 V ±0.05 V ABOVE VOL.

15	VOLIN1	Output linearity IIN1 = 1.05 IIN0	67.95	68.55	V
16	VOLIN2	Output linearity IIN2 = .95 IIN0	61.45	62.05	V
17	VOLIN3	Output linearity IIN3 = .90 IIN0	57.9	59.1	V
18	VOLIN4	Output linearity IIN4 = .80 IIN0	51.4	52.6	V
19	VOLIN5	Output linearity IIN5 = .60 IIN0	37.9	40.1	V
20	VOTC	Output voltage change with temperature	0	±1	V
21	VITR	Transient voltage input range	0	15	V
22	IITR	VITR = 15 V	0.4	0.95	mA
23	VIR	Pad voltage for IR = 1.0 mA	−1.6	−0.4	V
24	VOCL	Current limit bypass IIN = 0 mA VCC87 = 87 V	83.5	86.5	V

The following parameters apply to H853 and cannot be measured at die level.

25	Tr	Rise time IIN = 4IR CLOAD = 22 pF VOUT = 10% to 90%		≤15	ns
26	Tf	Fall Time IIN = 4IR CLOAD = 22 pF VOUT = 90% to 10%		≤25	ns
27	Abb	Aberrations VTR adjusted for optimum CLOAD = 15 pF	0	±10	%

APPLICATIONS INFORMATION

This circuit was designed to drive the Z-Axis and quadrapole electrodes of the T2503 CRT. All power supplies except the +87 V should be bypassed within 1 cm of the circuit with a high quality ceramic capacitor.

Care should be exercised that the output is not connected to a supply that is higher than the desired output. The current limiter protects the circuit only for a short to a voltage lower than the output.

A pullup resistor of 8k is required that will dissipate 0.64 W. A bootstrap capacitor of 22 pF is required to obtain a fast transient response. The current limiter is bypassed with 3300 pF. A 5.9k resistor from IREF to +5 V will set up 1 mA for the current sources.

The output should have at least 50 Ω in series with the capacitive load to preserve stable operation.

The current limiter will limit the circuit to a safe power dissipation during high amplitude sinusoidal outputs.

The stray capacitance on IIN should be less than 2 pF to preserve amplifier stability.

6

AUXILIARY PREAMPLIFIER DIE

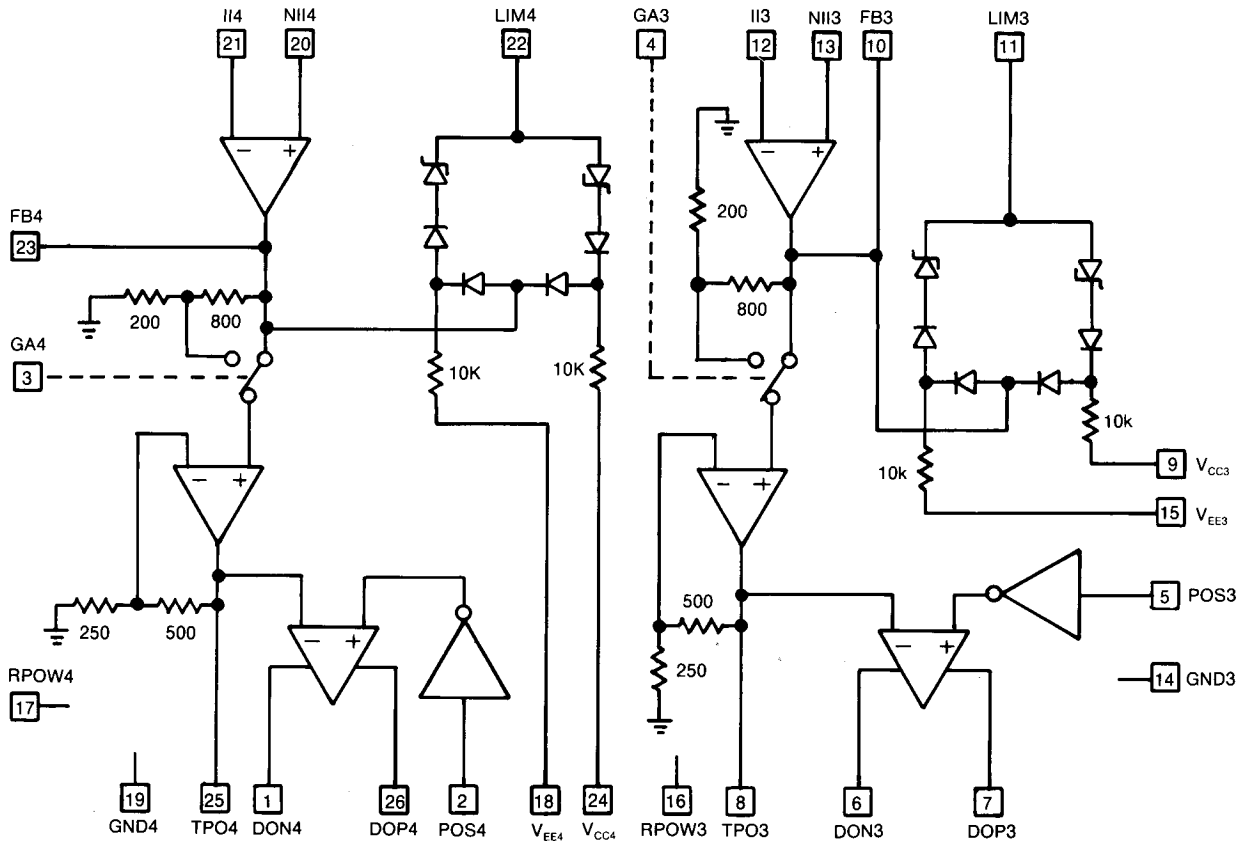
DESCRIPTION

The 203-0229-90 is a SHIII auxiliary preamplifier. It provides limited signal conditioning for two high-speed, high-impedance inputs when used with FET Impedance Converters.

FEATURES

- SHIII Process
- TTL Compatible Gain Switching
- Two Outputs per channel
  1. Single-ended without positioning for trigger pick off.
  2. Differential with positioning for display.
- On chip limiting for good overdrive recovery.

BLOCK DIAGRAM



ABSOLUTE MAXIMUMS

SYMBOLS	IDENTIFICATION	VALUE
T_J	Operating Junction Temperature	−15°C — +115°C
T_{STG}	Storage Temperature	−15°C — +125°C
V_{CC}	Positive Supply Maximum Voltage Range	−0.3 V — +7.0 V
V_{EE}	Negative Supply Maximum Voltage Range	+ 0.3 V — −7.0 V
$V_{(NII-II)}$	Maximum Differential Input Voltage NII or II (Pad 13 or 20 to Pad 12 or 21)	−2.5 V — +2.5 V
$V_{(NII)}$ $V_{(II)}$	Maximum Input Voltage, NII or II Pads (12 to 13 and 20 to 21)	VEE −0.3 V — +0.3 V
$V_{(LIM)}$	Maximum Input Voltage, LIM (Pads 11 and 22)	VEE −0.3 V — VCC +1.5 V
$V_{(GA)}$	Maximum Input Voltage, GA (Pads 3 and 4)	VEE −0.3 V — VCC +0.3 V
$V_{(POS)}$	Maximum Input Voltage, POS (Pads 2 and 5)	VEE −0.3 V — VCC +0.3 V
$V_{(RPOW)}$	Maximum Input Voltage, RPOW (Pads 16 and 17)	VEE −0.3 V — VCC +0.3 V

TERMINAL IDENTIFICATION

PAD #	NAME	FUNCTION	DESCRIPTION
1	DON4	Output	CH4 Display Output, Negative
2	POS4	Input	CH4 Position Input
3	GA4	Input	CH4 Gain Switch Control
4	GA3	Input	CH3 Gain Switch Control
5	POS3	Input	CH3 Position Input
6	DON3	Output	CH3 Display Output, Negative
7	DOP3	Output	CH3 Display Output, Positive
8	TPO3	Output	CH3 Trigger Pickoff Output
9	VCC3	Supply	CH3 +5 Volt Supply
10	FB3	Output	CH3 Feedback Output
11	LIM3		CH 3 Diode Limiter
12	II3	Input	CH3 Inverting Input
13	NII3	Input	CH3 Non-Inverting Input
14	GND3	Ground	CH3 Ground
15	VEE3	Supply	CH3 −5 Volt Supply
16	RPOW3	Bias	CH3 Bias Current
17	RPOW4	Bias	CH4 Bias Current
18	VEE4	Supply	CH4 −5 Volt Supply
19	GND4	Ground	CH4 Ground
20	NII4	Input	CH4 Non-Inverting Input
21	II4	Input	CH4 Inverting Input
22	LIM4		CH4 Diode Limiter
23	FB4		CH4 Feedback Out
24	VCC4	Supply	CH4 +5 Volt Supply
25	TPO4	Output	CH4 Trigger Pickoff Output
26	DOP4	Output	CH4 Display Output, Positive

ELECTRICAL CHARACTERISTICS

In the following summary refer to Figure 1 schematic for the following inputs and outputs:

V(IN) TTPO TDOP TDON V(FB) V(POS) V(GA)

NOTE: Power supply tolerances are ± 2% unless otherwise indicated.

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
1	V_{OFF}	Input Offset, NII-II	−10	+10	mV
2	I(II)	Bias Current, II	2.5	25	μA
3	AV(TTPO) (X1)	Voltage Gain (X1) V(GA) = Lo $\text{Gain} = \frac{V(TTPO)}{V(IN)}$	−1.55	−1.45	
4	AV(TTPO) (X0.2)	Voltage Gain (X0.2) V(GA) = Hi $\text{Gain} = \frac{V(TTPO)}{V(IN)}$	−0.310	−0.290	
4A	——	Ratio of X1 Output to X0.2 Output $\text{Ratio} = \frac{AV(TTPO,X1)}{AV(TTPO,X0.2)}$	4.90	5.10	
5	$V_{OM+(TTPO)}$	TTPO Output Positive Voltage Limit FB = +1 V V(GA) = "Lo"	0.50	0.80	V
6	$V_{OM\ (TTPO)}$	TTPO Output Negative Voltage Limit FB = −1 V V(GA) = "Lo"	−0.80	−0.50	V
7	$V_{OO(TTPO)}$	TTPO Change W/"Lo" − "Hi" Transition at V(GA) V(GA) = Pads 3 and 4	−10	+20	mV
8	AV(TDO, X.2)	Voltage Gain V(GA) = "HI" $\text{Gain} = \frac{V(TDOP) - V(TDON)}{V(IN)}$	0.580	0.620	
9	AV(TDO, X1)	Voltage Gain V(GA) = "Lo" $\text{Gain} = \frac{V(TDOP) - V(TDON)}{V(IN)}$	2.90	3.10	

ELECTRICAL CHARACTERISTICS (cont)

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
10	AV(TDO)	Common Mode Voltage Gain V(GA) = "Lo" $\text{Gain} = \frac{V(TDOP) + V(TDON)}{V(IN)}$	−0.150	0.150	
11	$V_{OO(TDO)}$	Differential Output Voltage V(TDOP) − V(TDON) V(FB) = 0 Volts V(GA) = "Hi" V(POS) = −2.5 Volts VCC = 5.0 Volts VEE = −5.0 Volts	−50	+50	mV
12	$V_{OC(TDO)}$	Common Mode Output Voltage V(FB) = 0 Volts V(GA) = "Hi" V(POS) = −2.5 Volts VCC = 5.0 Volts VEE = −5.0 Volts $V_{OC} = \frac{V(TDOP) + V(TDON)}{2}$	−50	+50	mV
13	$V_{OM+(TDO)}$	TDOP − TDON Maximum Positive Output Swing. V(FB) = 0 Volts V(POS) = −5 Volts Same pads as #11	450	650	mV
14	$V_{OM-(TDO)}$	TDOP − TDON Maximum Negative Output Swing V(FB) = 0 Volt V(POS) = 0 Volts Same pads as #11	−650	−450	mV
15	$V_{OM(TDO)MAX}$	TDOP − TDON Maximum Differential Output Swing. V(FB) = 0 Volts Change in V(POS) = +5 Volts	1.0	1.2	V
16	I_{LIM+}	LIM Input Current V(LIM) = +0.8 Volt V(FB) = 0 Volts	−5.0	+30	nA
17	I_{LIM-}	LIM Input Current V(LIM) = −0.8 Volt V(FB) = 0 Volts Pad 11	−30	+5.0	nA
18	I(GA)HI	GA Bias Current V(GA) = 2.4 Volts Pad 3 or 4	−10	+10	μA
19	I(GA)LO	GA Bias Current V(GA) = 0.4 Volt Pad 3 or 4	−0.5	0	mA

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ELECTRICAL CHARACTERISTICS (cont)

NUMBER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
20	V(GA)LO	GA Valid Data Range-LO Pad 3 or 4	−0.3	+0.8	V
21	V(GA)HI	GA Valid Data Range-HI Pad 3 or 4	2.0	VCC+.3	V
22	$V_{OC(POS)}$	POS Open Circuit Voltage Pad 5 or 2 VEE = −5.0 Volts	−2.6	−2.4	V
23	$Z_{I(POS)}$	POS Input Impedance Pad 5 or 2	10		KΩ
24	$V_{O(RPOW)}$	RPOW, Compliance Voltage Pad 16 or 17	−1.40	−0.60	V
25	$I_{EE(-5)}$	−5 Volts Supply Current Pad 18	−60	−45	mA

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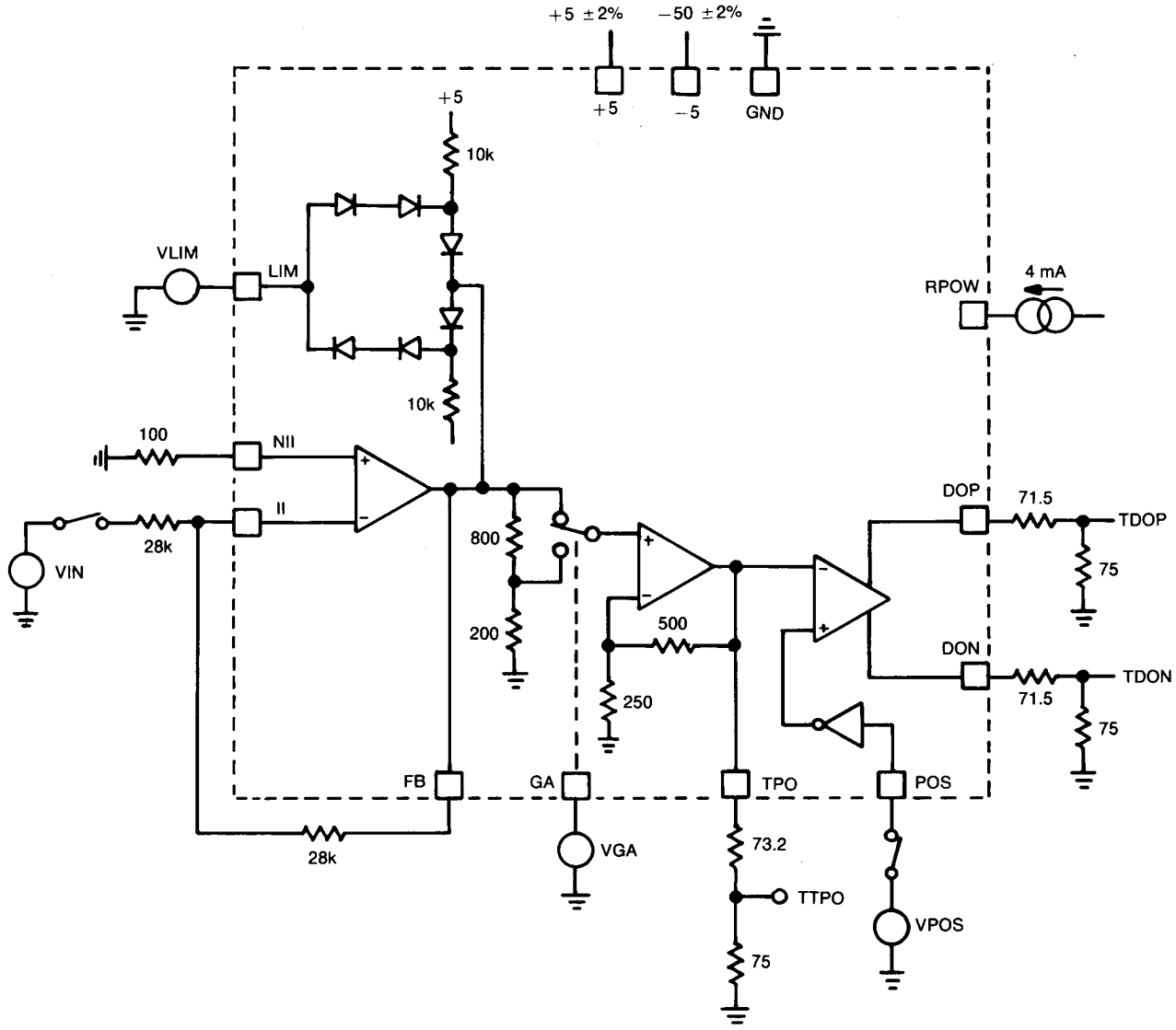
*1/2 M229A Autoprobe test conditions



APPLICATIONS INFORMATION

RELIABILITY

λ, failure rate $\leq$ 0.02%/1K Hours @ 75°C T_j

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SWEEP DAC DIE

DESCRIPTION

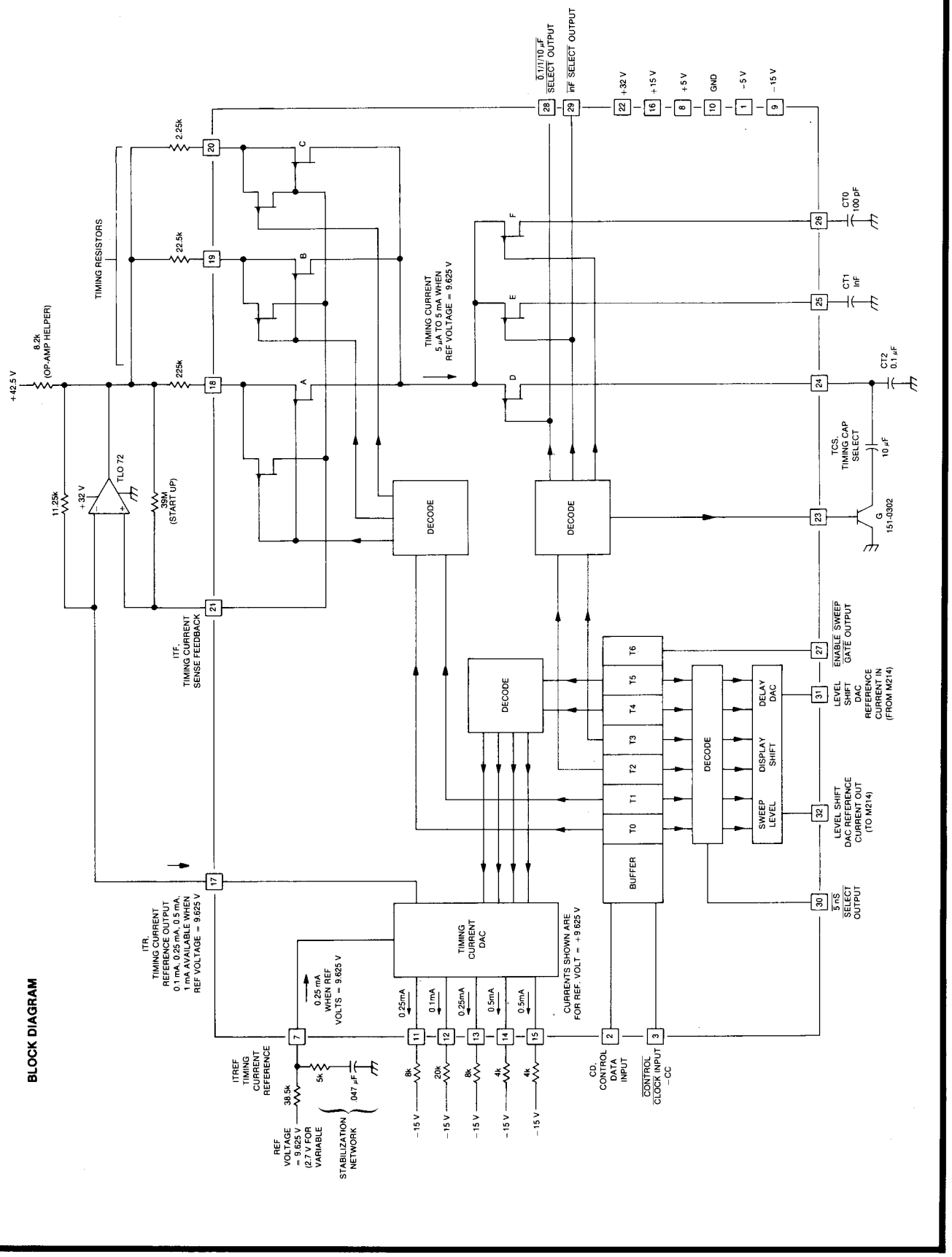
The 203-0231-90 is part of a sweep circuit system. This die contains circuitry for four separate functions as described under Features.

When used with the 203-0214-90 a complete sweep circuit system is generated with very few external components.

FEATURES

- 7 Bit Shift Register and buffer
- Programmable
- Timing Current Generator
- Timing Capacitor Select
- Sweep-Display Delay Level Shift DAC
- 200 Ω/sq BIFET Process

BLOCK DIAGRAM



ABSOLUTE MAXIMUMS

Symbols	Identification	Minimum	Maximum	Units
T_J	Operating Junction Temperature	−15	+125	°C
T_{STG}	Storage Temperature	−55	+150	°C
Pad 16	+15 Volts Voltage Range	−0.3	+18	V
Pad 9	−15 Volts Voltage Range	−18	+0.3	V
Pad 8	+5 Volts Voltage Range	−0.3	+7.0	V
Pad 1	−5 Volts Voltage Range	−7.0	+0.3	V
Pad 22	+32 Volt Supply Voltage Range	−0.3	+46	V
Pad 2	CD Input Voltage Range at Pad	−0.3	VCC5 + 0.3	V
Pad 3	−CC Input Voltage Range at Pad	−0.3	VCC5 + 0.3	V
Pad 7	ITREF Input Current Into Pad	0.0	400	μA
Pad 17	ITR Current Out Voltage Range at Pad	−0.3	VCC15 + 0.3	V
Pad 18	Timing Resistor Current Into Pad	0.0	100	μA
Pad 19	Timing Resistor Current Into Pad	0.0	1.0	mA
Pad 20	Timing Resistor Current Into Pad	0.0	10	mA
Pad 27, 28 29,30	Pads With Common Specs Current Out	−1.0	0.0	mA
Pad 31	LVL Shift "DAC" in Current Into Pad	0.0	1.5	mA
Pad 32	LVL Shift "DAC" Current Out Pad Voltage Range at Pad	VEE5 −0.3	+0.3	V

Table 1
ELECTRICAL REQUIREMENTS

(Refer also to Tables 3 and 4)

No.	Symbol	Conditions	Min	Max	Units
		POWER SUPPLY CURRENTS			
1	ICC32	+32 Volt Supply Current Range	1.50	4.55	mA
2	ICC15	+15 Volt Supply Current Range	2.00	6.00	mA
3	ICC5	+5 Volt Supply Current Range	18.0	45.0	mA
4	IEE5	−5 Volt Supply Current Range	−9.75	−2.00	mA
5	IEE15	−15 Volt Supply Current Range	−27.5	−6.0	mA
		LOGIC OUTPUT VOLTAGES REQUIRED TO INTERFACE WITH 203-0214-00 (Refer to Tables 3 and 4)			
6	$\overline{\text{ESG}}$-LO	Enable SWP GATE V-OUT (No Load) "LO" State	2.2	2.90	V
7	$\overline{\text{ESG}}$-HI	Enable SWP GATE V-OUT (No Load) "HI" State	3.36	3.8	V
8	$\overline{.1/1/10\ \mu\text{F SELECT}}$	V-OUT (No Load) "LO" State	2.2	2.90	V
9	$\overline{.1/1/10\ \mu\text{F SELECT}}$	V-OUT (No Load) "HI" State	3.31	3.8	V
10	$\overline{\text{1NF SELECT}}$	V-OUT (No Load) "LO" State	2.2	2.90	V
11	$\overline{\text{1NF SELECT}}$	V-OUT (No Load) "HI" State	3.31	3.8	V
12	VOUT HI(1 nF) −VOUT LO (.1/1/10 μf)	Calculated from tests 8-11	0.52		V
13	VOUT HI (.1/1/10 μF) −VOUT LO(1 nf)	Calculated from tests 8-11	0.52		V

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Table 1 (cont)

(Refer also to Tables 3 and 4)

No.	Symbol	Conditions	Min	Max	Units
14	VOUT HI (.1/1/10 μF) −VOUT HI(1 nf)	Calculated from tests 8-11	−0.12	+0.12	V
15	$\overline{\frac{5\text{ ns}}{\text{SELECT}}}$	VOUT (No Load) "LO" State	2.2	2.90	V
16	$\overline{\frac{5\text{ ns}}{\text{SELECT}}}$	VOUT (No Load) "HI" State	3.36	3.8	V
	TIMING CAPACITOR SELECT(TCS) OUTPUT REQUIREMENTS				
17	TCS(HI)	TCS Output Current "HI" State (into a 0.75 volt supply)	4.0	9.8	mA
18	TCS(LO)	TCS Output Voltage "LO" State	−2.5	−2.0	V
	Timing Current DAC-Offsets, Current Gain and Current Gain Ratios (See Table 2 for definition of terms.)				
19	M(1)	Current Gain (ITREF to ITR) (see Table 2)	1.99	2.01	
20	$\frac{M(OH)}{M(1)}$	Current Gain Ratio (see Table 2)	1.99	2.01	
21	$\frac{M(OL)}{M(1)}$	Current Gain Ratio (see Table 2)	1.99	2.01	
22	$\frac{M(2)}{M(1)}$	Current Gain Ratio (see Table 2)	0.4975	0.5025	
23	$\frac{M(3)}{M(1)}$	Current Gain Ratio (see Table 2)	0.199	0.201	
24	V(OH)	Offset (see Table 2)	−80	80	mV
25	V(OL)	Offset (see Table 2)	−80	80	mV
26	V(1)	Offset (see Table 2)	−80	80	mV
27	V(2)	Offset (see Table 2)	−80	80	mV
28	V(3)	Offset (see Table 2)	−80	80	mV

Table 1 (cont)

Sweep-Display Delay Level Shift DAC Output Current.
LSDRC (Pad 31) = 1.174 mA. LSDC Measured into −5 V Power Supply for the Following Shift Register T5,T0 Codes.

29	_____	T5,T0 = 000000	7.654	8.000	mA
30	_____	T5,T0 = 010000	3.82	4.01	mA
31	_____	T5,T0 = 100000	1.91	2.00	mA
32	_____	T5,T0 = 000001	759	807	μA
33	_____	T5,T0 = 000100	759	807	μA
34	_____	T5,T0 = 010001	370	412	μA
35	_____	T5,T0 = 010100	370	412	μA
36	_____	T5,T0 = 100001	176	215	μA
37	_____	T5,T0 = 100100	176	215	μA
38	_____	T5,T0 = 000010	61.7	94.8	μA
39	_____	T5,T0 = 000101	61.7	94.8	μA
40	_____	T5,T0 = 010101	−10	+10	μA
41	_____	T5,T0 = 100101	−10	+10	μA
42	_____	T5,T0 = 000110	−10	+10	μA
43	_____	T5,T0 = 010110	−10	+10	μA
44	_____	T5,T0 = 100110	−10	+10	μA
45	_____	T5,T0 = 110110	−10	+10	μA
46	_____	T5,T0 = 011001	−10	+10	μA
47	_____	T5,T0 = 011101	−10	+10	μA

INPUT BIAS VOLTAGES AND BIAS CURRENTS

48	_____	LSDRC input bias voltage 100 μA forced into pad 31	−15	−8.5	V
49	_____	Same as #49 Except force 1.5 mA into pad 31	−15	−8.5	V
50	_____	Control data bias current from 0.4 volt supply	−5	+5	μA
51	_____	Control data bias current from 2.4 volt supply	−5	+35	μA
52	_____	Not clock input bias current from 0.4 volt supply	−5	+35	μA
53	_____	Not clock input bias current from +2.4 volt supply	−5	+35	μA

Table 1 (cont)

Timing capacitor port fault catch voltages and "OFF" (port not selected) voltages. "OFF" voltage requirement will be "HI" or "LO" depending on timing capacitor selected (see Tables 3 and 4).

54	V-TC(3)	TC(3) (pad 26) fault catch voltage. CT0 selected. Timing current = 5 mA.	5.3	6.2	V
55	V-TC(2)	TC(2) (pad 25) fault catch voltage. CT1 selected. Timing current = 2.5 mA.	5.3	6.2	V
56	V-TC(1)	TC(1) (pad 24) fault catch voltage. CT2 selected. Timing current = 2.5 mA.	5.3	6.2	V
57	V-TC(1)	TC(1) (pad 24) voltage. "OFF" condition. "LO" state. CT0 selected. Force 10 μA into pad 24 and measure voltage at pad 24.	−1.2	−0.5	V
58	V-TC(2)	Same as #57 except pad 25	−1.2	−0.5	V
59	V-TC(3)	TC(3) (pad 26) voltage. "OFF" condition. "LO" state. CT1 selected. T5, T0 = 000100 Force 10 μA in pad 26 and measure pad 26 voltage.	−1.2	−0.5	V
60	V-TC(3)	TC(3) (pad 26) voltage. "OFF" condition. "LO" state. CT2 and TCS selected. T5, T0 = 001100 Force 10 μA into pad 26 and measure pad 26 voltage.	−1.2	−0.5	V
61	V-TC(1)	TC(1) (pad 24) voltage. "OFF" condition. "HI" state. CT1 selected. T5, T0 = 000100 Force 10 μA into pad 24 and measure pad 24 voltage.	5.3	6.0	V
62	V-TC(2)	TC(2) (pad 25) voltage. "OFF" condition. "HI" state. CT2 and TCS selected. T5, T0 = 001100 Force 10 μA into pad 25 and measure pad 25 voltage.	5.3	6.0	V

Table 1 (cont)

LEAKAGE CURRENT MEASURED AT TIMING CAPACITOR PORTS

63	Leakage. TR(1), CT2 and TCS selected. T5, T0 = 001110. Measure leakage current from pad 24 to 0 volt supply	−1.0	1.0	nA
64	Leakage Same as #63 except pad 24 to 3.85 volt supply.	−1.0	1.0	nA
65	Leakage. TR(1) and CT1 selected. T5, T0 = 000110 (pad 25 output). Measure leakage current from pad 25 to 0 volt supply.	−1.0	1.0	nA
66	Leakage Same as #65 except pad 25 to 3.85 volt supply.	−1.0	1.0	nA
67	Leakage TR(1) and CT0 selected. T5, T0 = 000010. Measure leakage current from pad 26 to 0 volt supply.	−1.0	10.	nA
68	Leakage Same as #67 except pad 26 to 3.85 volt supply	−10	10	nA

Table 1 (cont)

Large Current Errors—Compares current out at timing capacitor ports with current in at timing resistor ports

69	Large current error. TR(3) and CT0 selected. T5, T0 - 000000. Force 8.05 mA into pad 20. Measure current from pad 26 to +3.85 volt supply Calculate error: $\text{Error} = \frac{8.05\text{ mA} - \text{I(MEAS'D)}}{8.05\text{ mA}} \times 100\%$	−0.2	+0.2%	
70	Error @ pad 24. TR(3), CT2 and TCS selected. T5, T0 - 001100. Force 4.033 mA into pad 20. Measure pad 24 current to 3.85 volt supply Calculate error: $\text{Error} = \frac{4.033\text{ mA} - \text{I(MEAS'D)}}{4.033\text{ mA}} \times 100\%$	−0.2	+0.2	%
71	Error @ pad 25. TR(3) and CT1 selected. T5, T0 = 000100. Force 4.033 mA into pad 20. Measure current from pad 25 to 3.85 volt supply. Calculate error: $\text{Error} = \frac{4.033\text{ mA} - \text{I(MEAS'D)}}{4.033\text{ mA}} \times 100\%$	−0.2	+0.2	%
72	Current error @ pad 24. TR(2) and CT2 selected. T5, T0 = 001001. Force 805 μA into pad 19. Measure current from pad 24 to 3.85 volt supply. Calculate error: $\text{Error} = \frac{8.05\ \mu\text{A} - \text{I(MEAS'D)}}{805\ \mu\text{A}} \times 100\%$	−0.2	+0.2	%
73	Current error @ pad 25. TR(2) and CT1 selected. T5, T0 = 000101. Force 805 μA into pad 19. Measure current from pad 25 to 3.85 volt supply. Calculate error: $\text{Error} = \frac{805\ \mu\text{A} - \text{(IMEAS'D)}}{805\ \mu\text{A}} \times 100\%$	−0.2	+0.2	%

Table 1 (cont)

74	Error @ pad 24. TR(1), CT2, and TCS selected. T5, T0 = 001110. Force 81 μA into pad 18. Measure current from pad 24 to 3.85 volt supply Calculate error: $\text{Error} = \frac{81\ \mu\text{A} - (\text{IMEAS'D})}{81\ \mu\text{A}} \text{ X } 100\%$	−0.2	+0.2	%
75	Current error @ pad 25. TR(1) and CT1 selected. T5, T0 = 000110. Force 81 μA into pad 18. Measure current from pad 25 to 3.85 volt supply Calculate error: $\text{Error} = \frac{81\ \mu\text{A} - (\text{IMEAS'D})}{81\ \mu\text{A}} \text{ X } 100\%$	−0.2	+0.2%	
	Timing Current Sense Feedback (ITF) Continuity Check			
76	ITF continuity. TR(1) selected. T5, T0 = 000110. Ground pad 25. Force 10 μA in ITF (pad 21). Measure voltage pad 21 to pad 18. $\text{R(FET) ON} = \frac{\text{V(MEAS)}}{10\ \mu\text{A}}$	1	50	K
77	ITF continuity. TR(2) selected. T5, T0 = 000101. Ground pad 25. Force 15 μA in ITF (pad 21). Measure voltage pad 21 to pad 19. $\text{R(FET) ON} = \frac{\text{V(MEAS'D)}}{15\ \mu\text{A}}$	1	50	K
78	ITF continuity. TR(3) selected. T5, T0 = 000100. Ground pad 25. Force 45 μA in ITF (pad 21). Measure voltage pad 21 to pad 20. $\text{R(FET) ON} = \frac{\text{V(MEAS'D)}}{45\ \mu\text{A}}$	1	50	K

Table 1 (cont)

		CATCH DIODES			
79	V-ITF	ITF catch voltage 43K resistor hooked from ITF (pad 24) to gnd. T5, T0 = 111110. Pads 18, 19, and 20 open. Measure voltage at ITF.	3.9	4.5	V
80	V-ITR	ITR catch voltage Force 0.2 mA into ITR (pad 17) T5, T0 = 111110. Measure voltage at ITR.	15.2	16.2	V
		FET PARAMETERS			
81	VP	FET pinchoff voltage Drain voltage = −8 V Drain current = −1 μA	1.0	5.0	V

Table 2
Measurements and Calculations Made to Determine Current Gain, Current Gain Ratios, and Offset of Timing Current DAC

Measure	Shift Register Code T5, T4	A 38.5K Resistor Connected Between ITREF (Pad 7) and VR. VR as Follows	Voltage at Pad 17
ITRA(1)	01	9.0 V	15 V
ITRB(1)	01	2.7 V	15 V
ITRA(OH)	00	9.0 V	15 V
ITRA(OL)	00	9.0 V	7.5 V
ITRB(OH)	00	2.7 V	15 V
ITRB(OL)	00	2.7 V	7.5 V
ITRA(2)	10	9.0 V	15 V
ITRB(2)	10	2.7 V	15 V
ITRA(3)	11	9.0 V	15 V
ITRB(3)	11	2.7 V	15 V

$$\text{CALCULATE: } M(X) = \frac{38.5K(ITRA(X) - ITRB(X))}{9 - 2.7}$$

$$\text{CALCULATE: } V(X) = \frac{9ITRB(X) - 2.7ITRA(X)}{ITRA(X) - ITRB(X)}$$

Where X = OH, OL, 1, 2, 3

NOTE 1: M(X) = Current Gain

NOTE 2: V(X) = Offset

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Table 3
Truth Table*
Output and Timing Resistor Port Levels

Shift Register Code T6, T0	ITR	TR(1)	TR(2)	TR(3)	
–00----	1 mA				
–01----	0.5 mA				
–10----	0.25 mA				
–11----	0.1 mA				
----00		CLP	CLP	SEL	
----01		CLP	SEL	CLP	
----10		SEL	CLP	CLP	

Table 4
Truth Table
Output and Timing Capacitor Port Levels

Shift Register Code T6, T0	TCS	CT2	CT1	CT0	Not ESG	Not 0.1 μF, 1 μF, 10 μF, SEL	Not 1 nf SEL	Not 5 nS SEL
---00--	LO	LO	LO	SEL		HI	HI	
---01--	LO	HI	SEL	LO		HI	LO	
---10--	LO	SEL	HI	LO		LO	HI	
---11--	HI	SEL	HI	LO		LO	HI	
1-----					LO			
0-----					HI			
-000000								LO
-All other								HI

Tables 3 and 4 Notes:

1. **Nominal ITR current with 9.625 V and 38.5K at ITREF.**
2. **SEL = selected**
3. **CLP = clamped**
4. **Shift register inputs at CD and –CC are TTL.**
   a. **VIL(MAX) = 0.8 V**
   b. **VIH(MIN) = 2.0 V**
5. **ITF output always senses voltage at bottom of selected timing resistor.**
6. **See Tests 29 through 47 for LSDRCO output truth table.**
7. **Data from the "CONTROL DATA" input, shifts into the control register (appears at register true outputs) at "NOT CONTROL CLOCK" low to high transitions, bit 6 first and bit 0 last. "Not Control Clock" must be maintained high after last shift to prevent false register oututs.**

Table 5
Terminal Identification

Pad #	Name	Input/Output	Description
1	VEE5	Supply	−5 Volt Supply
2	CD	Input	Control Data
3	−CC	Input	Not Control CLK IN
4			Test FET
5			Test FET
6			Test FET
7	IT-REF	Input	Timing Current Reference
8	VCC5	Supply	+5 Volt Supply
9	VEE15	Supply	−15 Volt Supply
10	GND		Ground
11	TCDR (1)	Input	Timing current DAC Resistor
12	TCDR (2)	Input	Timing current DAC Resistor
13	TCDR (3)	Input	Timing current DAC Resistor
14	TCDR (4)	Input	Timing current DAC Resistor
15	TCDR (5)	Input	Timing current DAC Resistor
16	VCC15	Supply	+15 Volt Supply
17	ITR	Output	Timing Capacitor Ref. Output
18	TR (1)		Timing Resistor
19	TR (2)		Timing Resistor
20	TR (3)		Timing Resistor
21	ITF	Output	Timing Current Sense Feedback Output
22	VCC32	Supply	+32 Volt Supply
23	TCS	Output	Timing Capacitor Select
24	CT2 .1 μF, 1 μF, 10 μF		Timing Capacitor
25	CT1 1 nF		Timing Capcitor
26	CT0 100 pF		Timing Capacitor
27	Not ESG	Output	Not Enable Sweep Gate Output
28	0.1, 1, 10 μF Not Select	Output	Capcitor Not Select Output
29	1 nF Not Select	Output	Capacitor Not Select Output
30	5 nS Not Select	Output	Capacitor Not Select Output
31	LSDRC	Input	Level Shift DAC Ref Current In
32	LSDC	Output	Level Shift DAC Current Out

Applications Information

7-Bit Shift Register (see Tables 3 and 4)

Operation of the sweep circuit system is programmed by clocking a 7-bit code into this register. Parallel outputs are decoded and used to control the various functions of the 203-0231 and the 203-0214. Two of the bits program the timing current DAC, two of the bits select the timing resistor, and two of the bits select the timing capacitor. The seventh bit controls the Enable Sweep Gate function and is sent directly to the 203-0214-00 as "Not Enable Sweep Gate". A "One" at T6 (Enable Sweep Gate) of the register will allow "Not Sweep Gate Output" from the 203-0214-00 during sweep. A "Zero" on T6 inhibits "Not Sweep Gate" outputs.

Timing Current Generation

When combined with 10 off chip accurate resistors (9 of them are trimmed thick film on the H851 substrate) and an external op-amp, the 203-0231 provides a current (digitally programmed) that ranges from 5 microamps to 5 milliamps in a 5, 12.5, 25, 50, 125, etc., sequence. This current can be steered, with limitations, to one of three outputs corresponding to the three timing capacitor ports. The limitations referred to are the maximum current that can flow out of the three ports. The 100 pF port can handle the full 5 mA, the 1 nF port can handle 2.5 mA. The 0.1 μF, 1 μF, 10 μF port can handle up to 2.5 mA.

The timing current (5 microamps to 5 milliamps) is generated in two stages. The process is as follows. A reference voltage (9.625 V) is applied to one end of a 38.5K resistor. The other end of the resistor is attached to the reference input (Pad 7-ITREF) of the timing current DAC. An internal op-amp keeps Pad 7 at zero volts and hence the reference current is approximately 0.25 mA. Scope "Variable Sweep Speed" is obtained by reducing the 9.625 V reference.

Output (ITR) of the timing current DAC is 0.1 mA, 0.25 mA, 0.5 mA, or 1 mA depending on the input digital code.

Shift register bits T4 and T5 contain the programming information for the timing current DAC. Timing current DAC output (ITR) is mirrored and multiplied by the network consisting of the external op-amp, the timing resistors, and FETS A, B, and C.

Shift register bits T0 and T1 contain the timing resistor select information.

Timing Capacitor Select (Refer to the Block Diagram)

The timing current (5 μA to 5 mA) is now steered to the appropriate timing cap port by FETS D, E, and F.

Shift register bits T2 and T3 contain the timing cap port select information. When the timing cap select (TCS) output from the 203-0231 and an external transistor (G) are used, a four timing capacitor system is realized.

Sweep-Display Delay Level Shift DAC (Refer to the Block Diagram)

See explanation in 203-0214-00 for a description of how the delay function works.

The level shift DAC in the 203-0231 requires a reference current which is supplied by the 203-0214. Max current from the level shift DAC occurs when the 5 ns/div sweep speed is selected. Under this condition the current out of the level shift DAC is 6.667 times the reference current.

At 10 ns/div the current out of the level shift DAC is 1/2 of the maximum. At 20 ns/div the current out of the level shift DAC is 1/4 of the maximum. At 50 ns/div the current out of the level shift DAC is 1/10 of the maximum. Output current continues to decrease in this manner for sweep speeds of 5 ns/div through 500 ns/div.

For sweep speeds of 1 μs/div and slower the current out is zero.

6

COST

7

7

COSTING

TRANSFER COSTS FOR NEW USAGE OF AN EXISTING MONOLITHIC PACKAGED PART

If you are planning to use an existing monolithic packaged part in a new instrument design, please call ICM Applications Engineering (phone 627-1037). A significant increase in existing monolithic part volume may change the equipment required to manufacture it and it may affect the transfer cost.

Projected transfer costs up to 4 years beyond the present Fiscal Year can be obtained through a formal request to ICM Applications Engineering.

It is recommended that component use decisions for new applications of existing components be based on incremental cost (sometimes called variable cost). Variable cost is the labor, material, and variable burden portions of the transfer cost. Overhead (fixed cost) is subtracted and the incremental cost with yield loss is derived.

Incremental cost information also can be obtained by a formal request through ICM Applications Engineering.

More information on costing policies and definitions can be obtained from your Division cost accountant.

Fully burdened transfer costs are available from ICM Applications Engineering. They include yield loss and all overhead (fixed cost), and are reviewed quarterly and adjusted when appropriate.

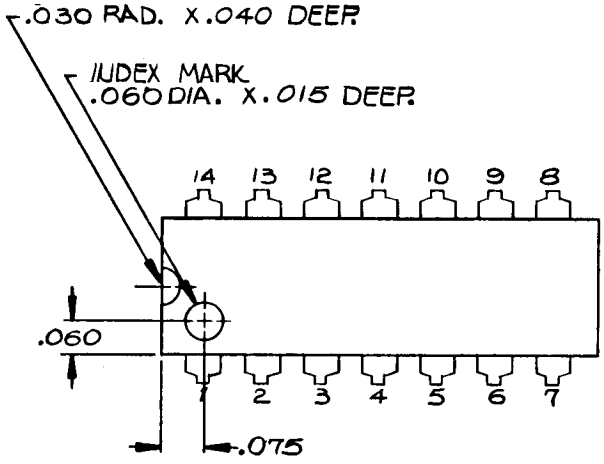
7

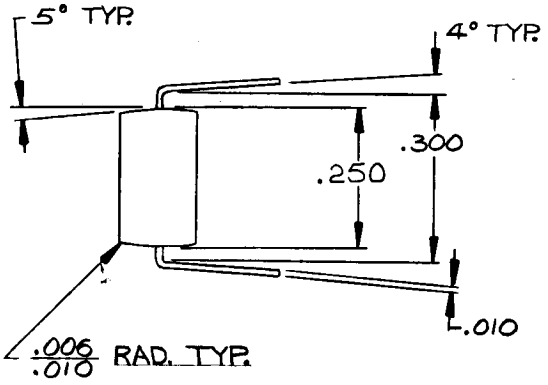
PACKAGE INFORMATION

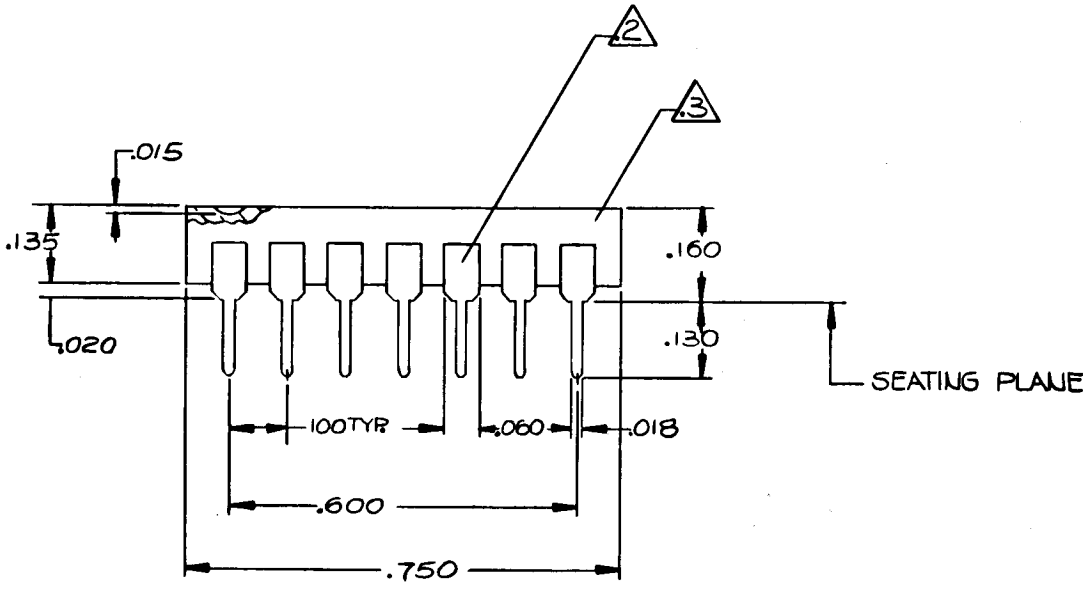
8

8

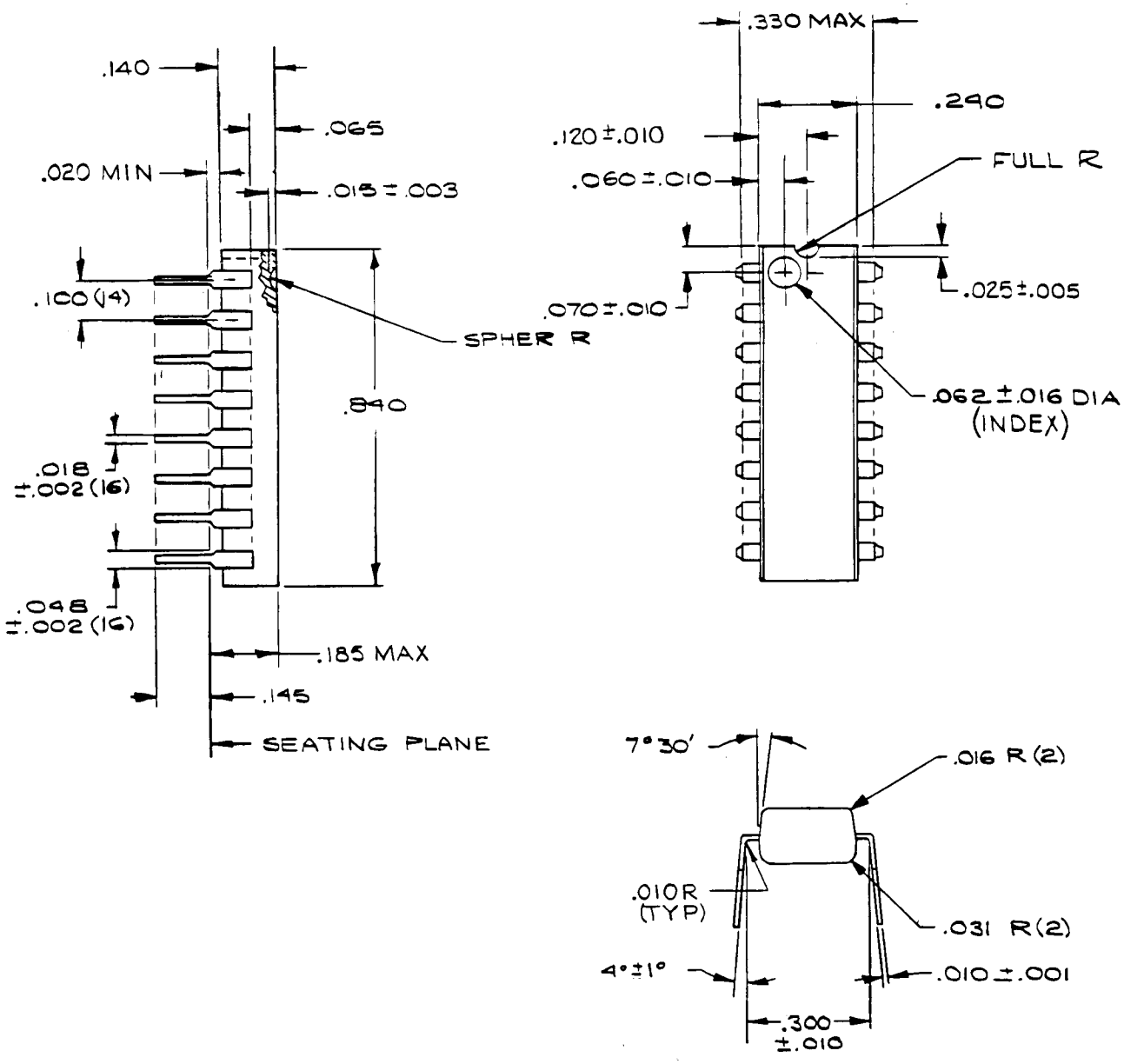
14 PIN DIP


.030 RAD. X .040 DEEP
INDEX MARK
.060 DIA. X .015 DEEP
14 13 12 11 10 9 8
.060
1 2 3 4 5 6 7
.075

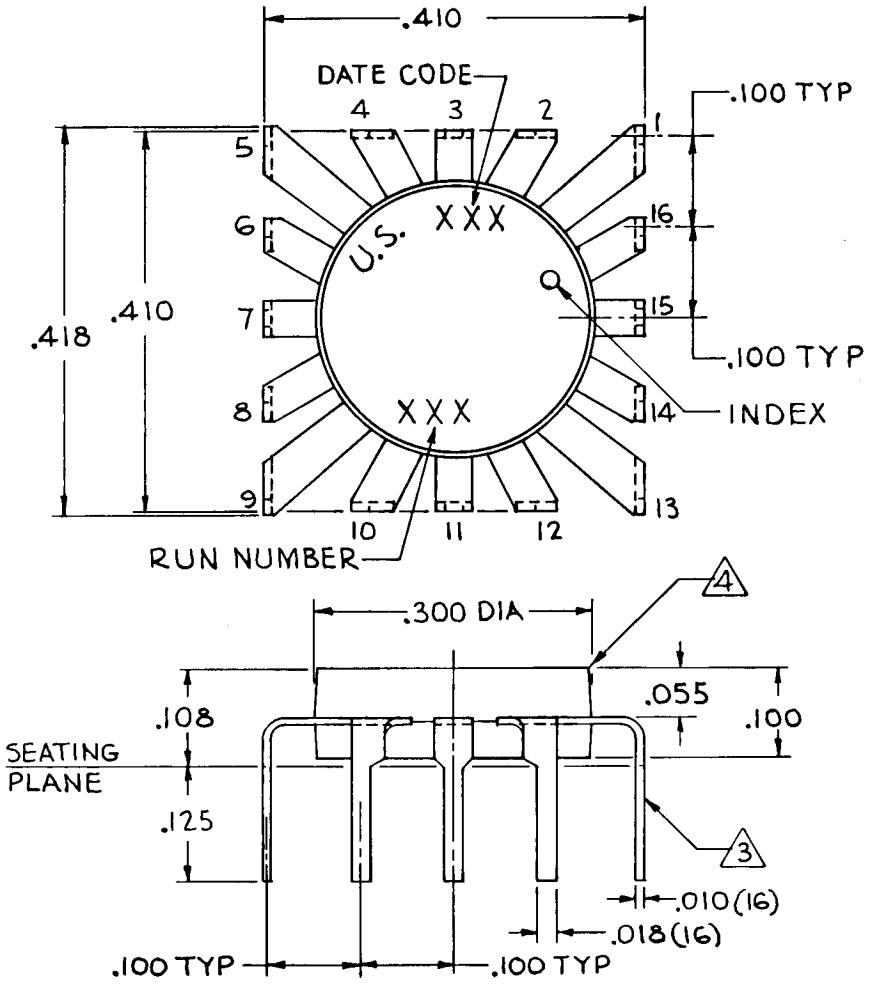

5° TYP.
4° TYP.
.300
.250
.010
.006
.010
RAD. TYP.


.2
.3
.015
.135
.020
.160
.130
SEATING PLANE
.100 TYP.
.060
.018
.600
.750

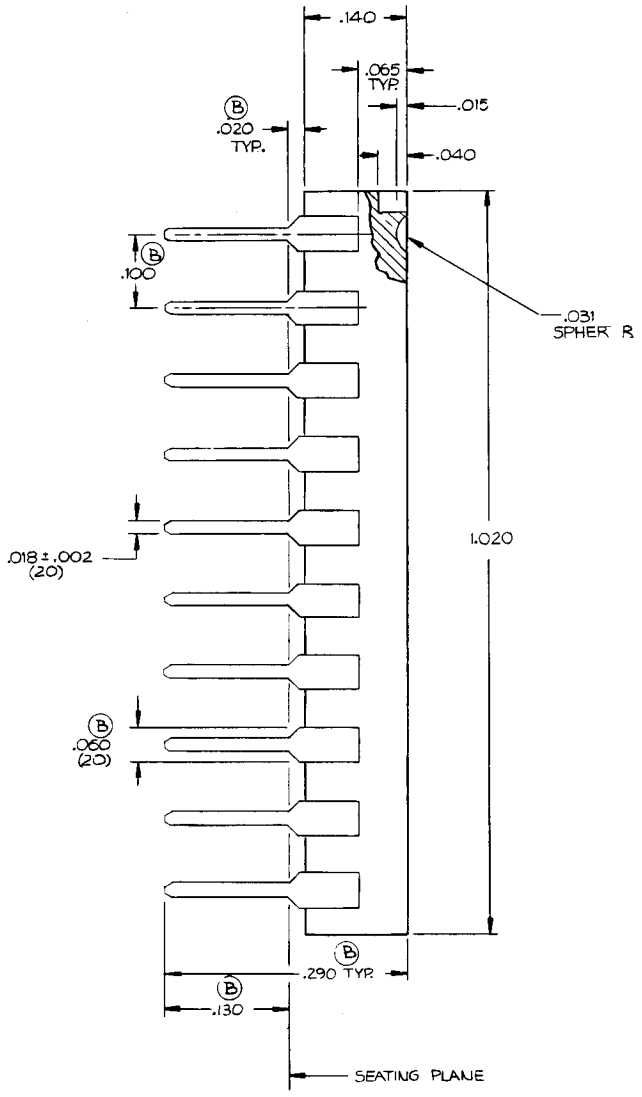
16 PIN DIP

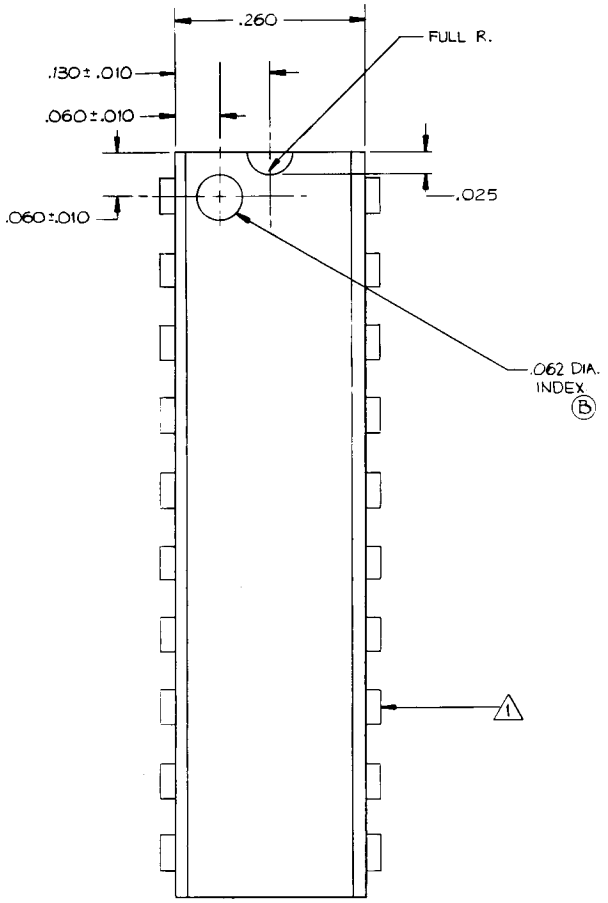

.140
.065
.020 MIN
.015 ± .003
.100 (14)
SPHER R
.840
.018 ±.002 (16)
.048 ±.002 (16)
.185 MAX
.145
SEATING PLANE
.330 MAX
.290
.120 ±.010
.060 ±.010
FULL R
.025 ±.005
.070 ±.010
.062 ±.016 DIA (INDEX)
7°30'
.016 R (2)
.010R (TYP)
.031 R(2)
4° ±1°
.010 ±.001
.300 ±.010

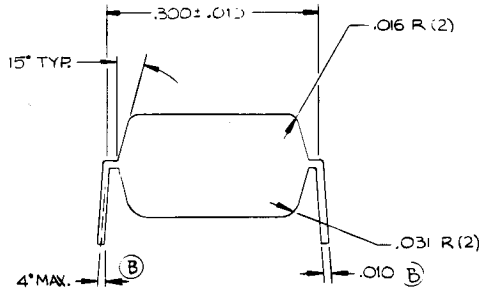
16 PIN MINI PAC



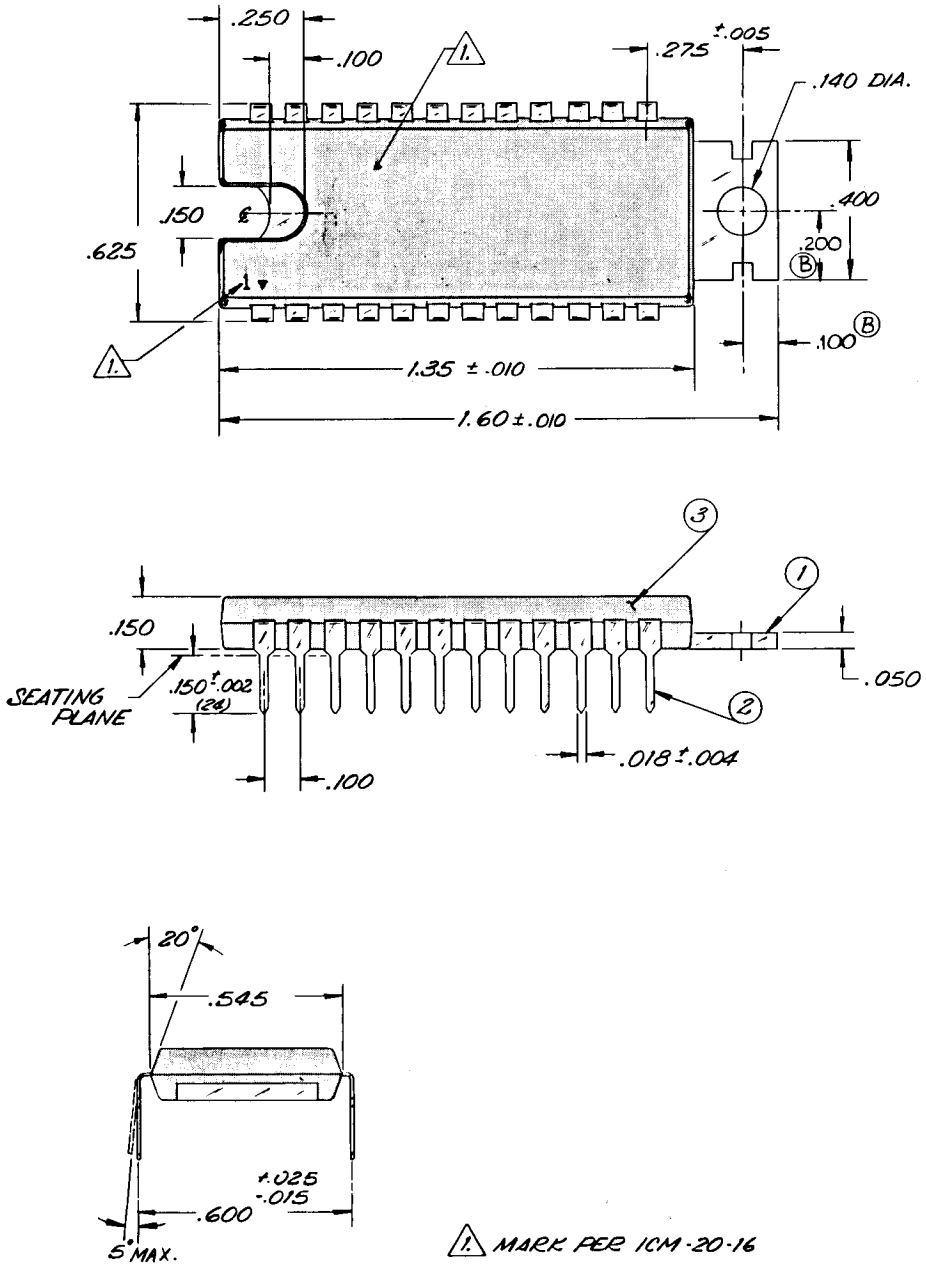
20 PIN DIP


.140
.065 TYP.
.015
.020 TYP.
.040
.100
.031 SPHER R
1.020
.018±.002 (20)
.060 (20)
.290 TYP.
.130
SEATING PLANE

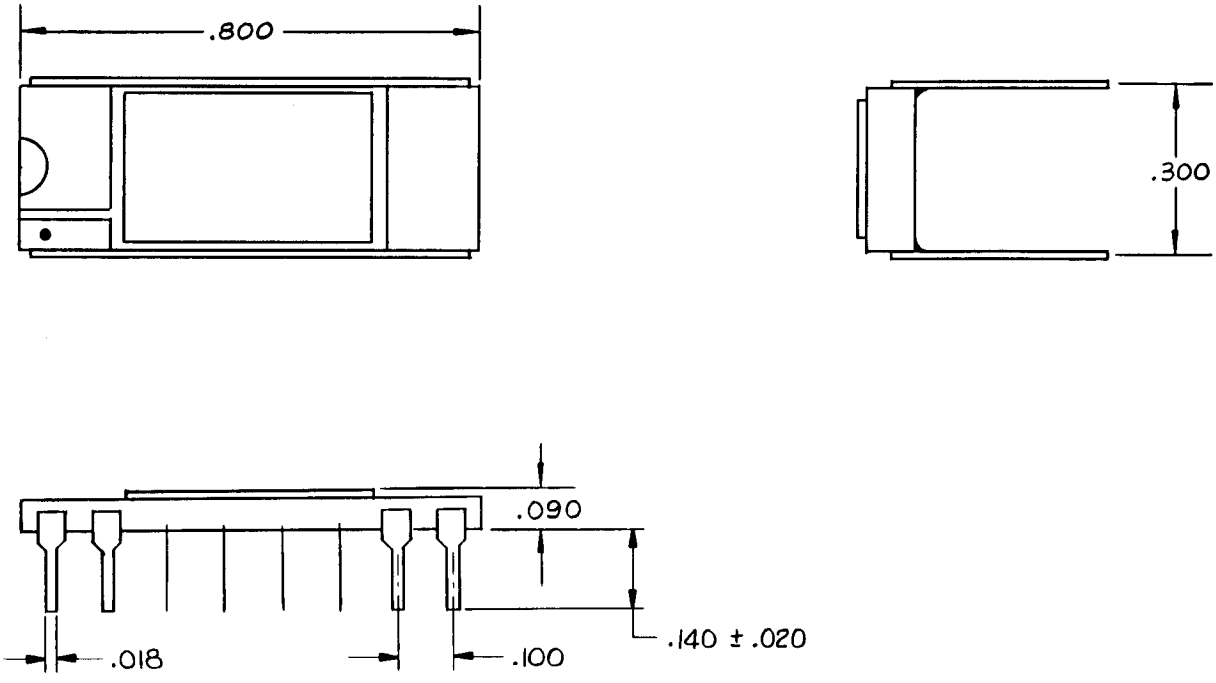

.260
FULL R.
.130±.010
.060±.010
.060±.010
.025
.062 DIA. INDEX
1


.300±.010
.016 R (2)
15° TYP.
.031 R (2)
4° MAX.
.010

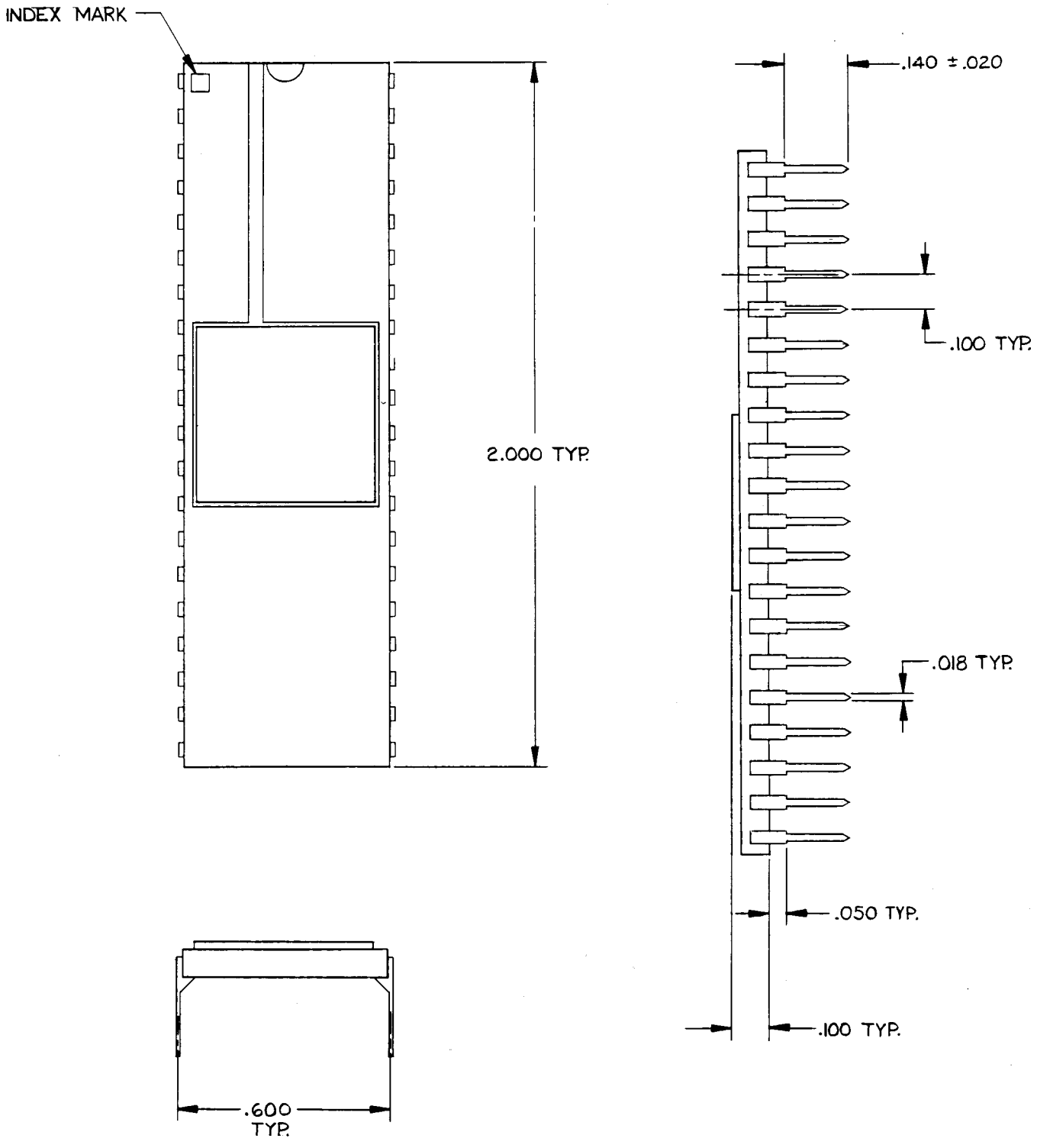
24 PIN POWER PLASTIC



16 PIN CER



40 PIN CER


INDEX MARK
2.000 TYP.
.600
TYP.
.140 ± .020
.100 TYP.
.018 TYP.
.050 TYP.
.100 TYP.

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